20W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

FEATURES

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V~17V
- Up to 20W Power Transfer
- Integrated Full-Bridge Power Stage with 13-mΩ Rdson of Power MOSFETs
- Integrated High Efficiency 5V-1A Step-down DC/DC Converter
- Optimized for EMI Reduction
- Build-in 3.3V-200mA LDO
- Provide 2.5V Voltage Reference
- Integrated Lossless Input Current Sensor with ±2% accuracy for FOD and current Demodulation
- 3.3V and 5V PWM Signal Logic Compatible
- Input Under-Voltage Lockout
- Over Current Protection
- Over Temperature Protection
- 3mm*4mm QFN-19L Package

APPLICATIONS

- WPC Compliant Wireless Chargers of 5W to 15W Systems for Mobiles, Tablets and Wearable Devices
- General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
- Proprietary Wireless Chargers and Transmitters

DESCRIPTION

The SCT63240 is a highly integrated Power Management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system compliant with WPC specification to support up to 20W power transfer, working with a wireless application specific controller or a general MCU based transmitter controller.

This device integrates a 4-MOSFETs full bridge power stage，gate drivers, a 5V step-down DC/DC converter, a 3.3V LDO, a 2.5V accurate voltage reference and input current sensor for both system efficiency and easy-to-use.

The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The proprietary lossless current sensing circuitry with ±2% accuracy monitors input current of full bridge to support Foreign Object Detection FOD and current demodulation. The build-in 5V step-down DC/DC converter and 3.3V low dropout regulator LDO can provide power supplies to transmitter controller and external circuitries.
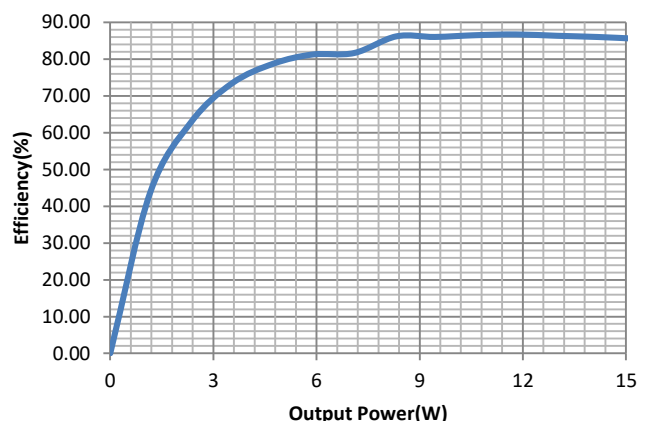
The SCT63240 features input Under-Voltage Lock-out UVLO, over current, short circuit protection, and over temperature protection.

The SCT63240 is available in a compact 3mm*4mm QFN package.

TYPICAL APPLICATION
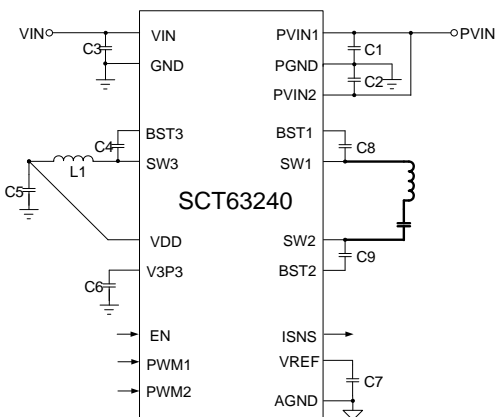
Power Transfer Efficiency with 15W RX @ Vout=12V

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SCT63240

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT63240FIA[1]	3240	QFN-19L

(1) For Tape & Reel, Add Suffix R (e.g. SCT63240FIAR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted[1]

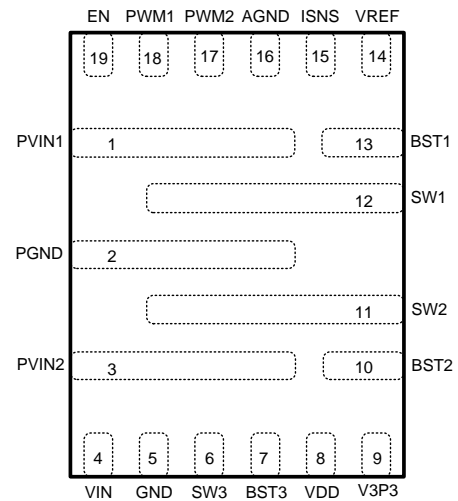| DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	20	V
SW1,SW2	-1	20	V
SW3	-1	24	V
BST1,BST2	-0.3	26	V
BST3	-0.3	30	V
BST1-SW1,BST2-SW2,BST3-SW3	-0.3	6	V
VDD, V3P3, VREF, ISNS, EN, PWM1, PWM2	-0.3	6	V
Operating junction temperature TJ[2]	-40	125	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

Figure 1. Top view 19-Lead QFN 3mm*4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	2	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	3	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q1. Local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
VIN	4	Input supply voltage of the Buck converter. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	5	Power ground of the Buck converter.
SW3	6	Switching output of the Buck converter. Connect SW3 to an external power inductor.

BST3	7	Power supply bias for the high-side power MOSFET gate driver of Buck converter. Connect a 0.1uF capacitor from BST3 pin to SW3 pin.
VDD	8	Output voltage of the Buck converter. Connect 22uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage, the 3.3V LDO and the 2.5V voltage reference.
V3P3	9	3.3V LDO output. Connect 1uF capacitor to ground.
BST2	10	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	11	Switching node of the half-bridge FETs Q3 and Q4.
SW1	12	Switching node of the half-bridge FETs Q1 and Q2.
BST1	13	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VREF	14	Output of the 2.5V LDO. Connect a 1uF capacitor to ground.
ISNS	15	Current detection output. The voltage of the pin is proportional to the input current.
AGND	16	Analog ground of the IC
PWM2	17	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off.
PWM1	18	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off.
EN	19	Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, Buck converter will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to PWM input logic then.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	20	V
P_{VIN}	Input voltage range	1	17	
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins[1]	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins[2]	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance[1]	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[1]	45	

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(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63240 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{PVIN1}=V_{PIN2}=12V$, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		17	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		3.6 400		V mV
V_{DD_UVLO}	V_{DD} UVLO Threshold Hysteresis	V_{DD} rising		3.8 440		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	µA
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I_{SHDN_VDD}	Shutdown current from VDD	EN=0V, VDD=5.5V		18	35	uA
I_{VINQ}	Quiescent current from VIN pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		210		uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		50		uA
I_Q	Quiescent current from VDD pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		270		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
V_{IH}	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.65			V
V_{IL}	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.55	V
V_{TS}	PWM1, PWM2 Tri-state voltage		1.2		2	V
Power Stage						
R_{DSON_Q1}	High-side MOSFETQ1 on-resistance	V_{BST1}-V_{SW1}=5V		13		mΩ
R_{DSON_Q2}	Low-side MOSFETQ2 on-resistance	VDD=5V		13		mΩ
R_{DSON_Q3}	High-side MOSFETQ3 on-resistance	V_{BST2}-V_{SW2}=5V		13		mΩ
R_{DSON_Q4}	Low-side MOSFETQ4 on-resistance	VDD=5V		13		mΩ
I_{LIM}	How-side current limit threshold			12.5		A
Buck converter						
F_{SW}	Switching frequency		540	600	660	KHz
V_{DD}	Output voltage		4.925	5	5.075	V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold			1.5		A
T_{HIC_W}	Over current protection hiccup wait time			0.85		ms

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{HIC_R}	Over current protection hiccup restart time			27		ms
R_{DSON_H}	High side FET on-resistance			380		mΩ
R_{DSON_L}	Low side FET on-resistance			200		mΩ
T_{SS}	Internal soft-start time			2		ms

3.3V LDO

V_{3P3}	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I_{3P3}	Output current Capability			200		mA
I_{SC1}	Short current			50		mA

2.5V REFFERENCE OUTPUT

V_{2P5}	Output voltage reference	Cout=1uF, VDD=5V	2.475	2.5	2.525	V
I_{3P3}	Output current Capability			100		mA
I_{SC2}	Short current			40		mA

Current Sense

V_{ISNS0}	Voltage with no input current	I_{PGND}=0A ,Tj=25℃ PWM1=PWM2=0V	0.585	0.6	0.615	V
R_{ISNS}	Input current to output voltage gain	$V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}$	0.98	1	1.02	V/A
V_{ISNS1}	Voltage with 0.6A input current	I_{PVIN}=0.6A, Tj=25℃	1.176	1.2	1.224	V
V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25℃	1.568	1.6	1.632	V

Protection

T_{SD}	Thermal shutdown threshold	T_J rising		155		°C
	Hysteresis			35		°C

TYPICAL CHARACTERISTICS
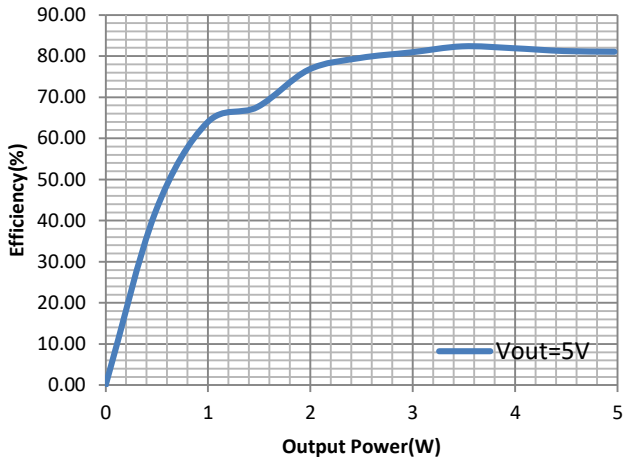
Figure 2. Transfer Efficiency with 5W RX@ Vout=5V
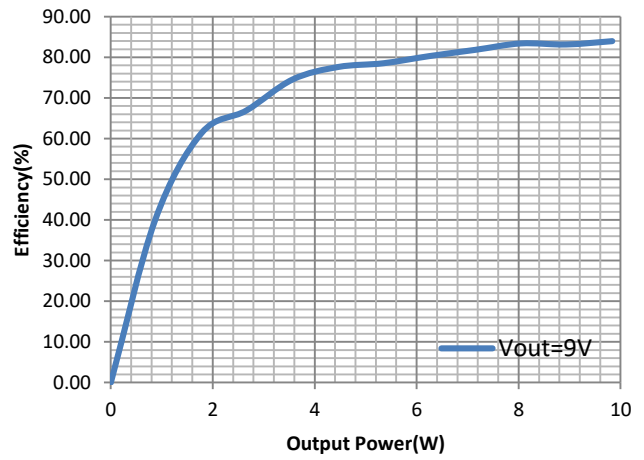
Figure 3. Transfer Efficiency with 10W RX@ Vout=9V
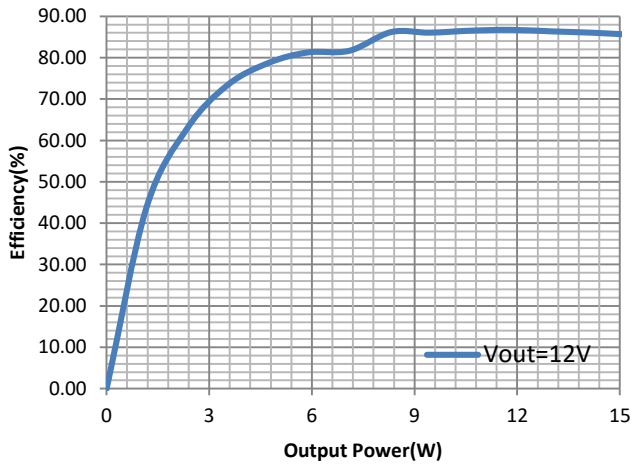
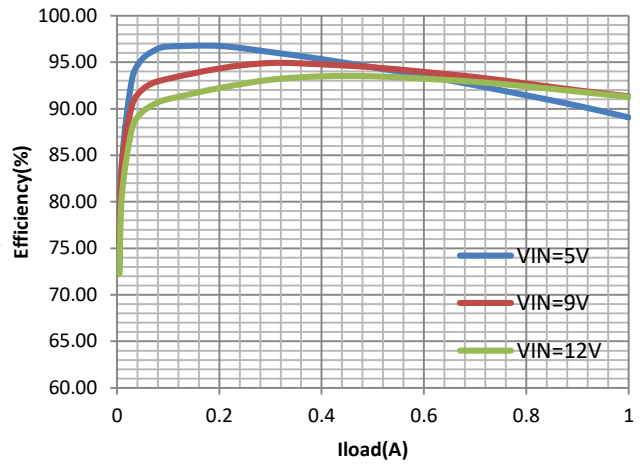Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

Figure 5. Buck Converter Efficiency

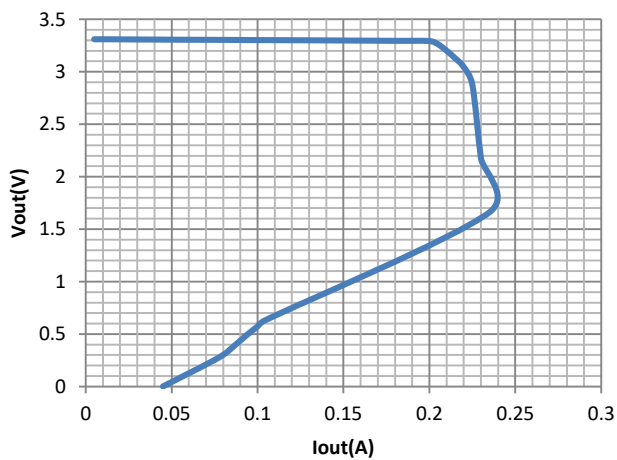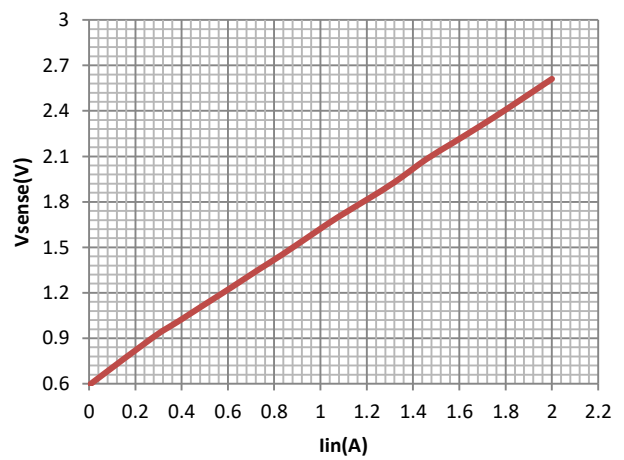Figure 6. 3.3V LDO Iout vs Vout

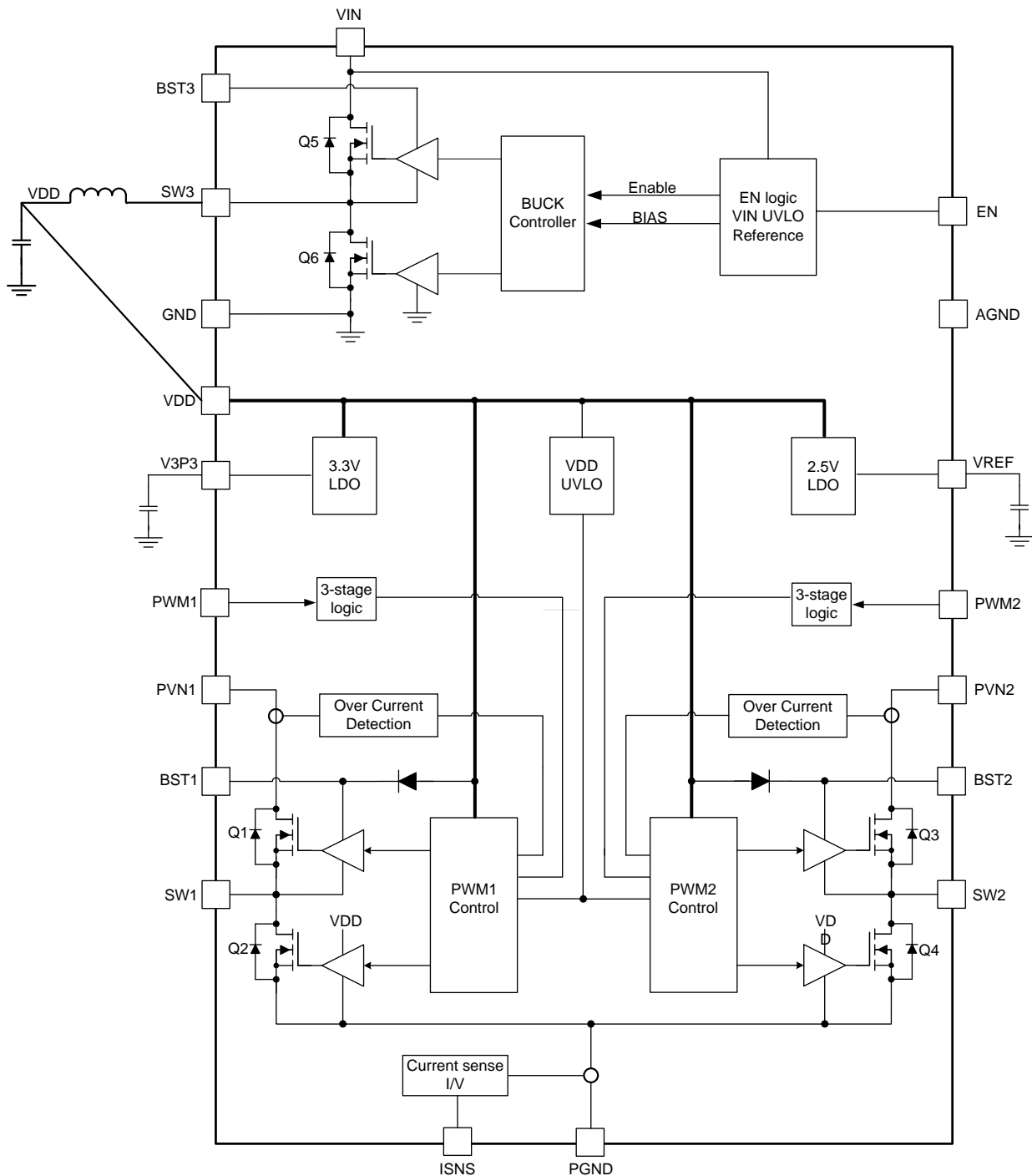Figure 7. Current Sense Output Voltage vs Iin

FUNCTIONAL BLOCK DIAGRAM

Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT63240 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V buck converter as power supply for external transmitter controller and internal 5V power supply to increase system efficiency, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU and a 2.5V reference voltage.

The SCT63240 has four power input pins. VIN is connected to the power FETs of buck converter. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer. VDD is the output feedback pin of the 5V output buck converter and at the mean while as the power supply for internal two LDOs and full bridge MOSFET's gate driver.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 17V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63240 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The buck converter and full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63240 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for buck converter and 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the buck converter and two LDOs enable at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after buck converter works, and also the V3V and VREF output do. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider(R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.18 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \qquad (1)$$

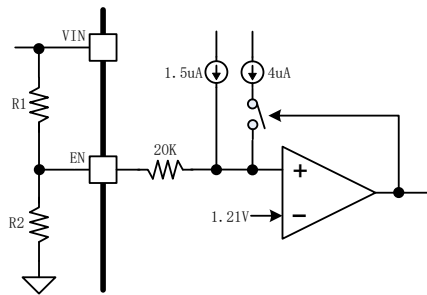$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 5.5uA * R1 \qquad (2)$$

Figure9. System UVLO by enable divider

5V Output Buck Converter

The SCT63240 fully integrates synchronous buck converter with up to 20V input voltage and 5V fixed output voltage, which offers up to 1A output current capability. The device employs 600KHz fixed frequency peak current mode control with the internal loop compensation network and built-in 2ms soft-start which makes this buck converter easily to be used by minimizing the off-chip component count. Pulse Skipping Modulation(PSM) is adopted to improve the light load efficiency.

The buck converter's output, a fixed 5V voltage, supports the power requirement on system such as transmitter controller or mechanical fan meanwhile it is also the power supply of the SCT63240's 3.3V LDO, VREF LDO and gate drivers of 4-MOSFETs full bridge. Connect 22uF capacitor from VDD to GND and add a 0.1uF local bypass ceramic capacitor placed close to the IC.

The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

An external 100nF ceramic bootstrap capacitor between BST3 and SW3 pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Buck converter implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When output voltage under regulation lasts for 850 us, the converter stops switching; After remaining OFF for 13.6 ms，the device will attempt to restart from soft-start.

The hiccup protection mode above greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

Full bridge and PWM Control

The SCT63240 integrate full bridge power stage with only 13mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

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Full Bridge Over Current Protection

The SCT63240 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63240 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1V/A. The equation 3 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

$$V_{ISNS} = 600mV + I_{PGND} * 1V/A \qquad (3)$$

3.3V LDO

The SCT63240 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 200mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

VREF Voltage Reference Output

The SCT63240 also has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 2.5V voltage on VREF pin. The accuracy of the VREF voltage is ±1% and output current capability is 100mA . This voltage regulator can be used as the supply voltage or a reference voltage to external IC and circuit.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VREF pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Thermal Shutdown

The SCT63240 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops Buck converter, two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

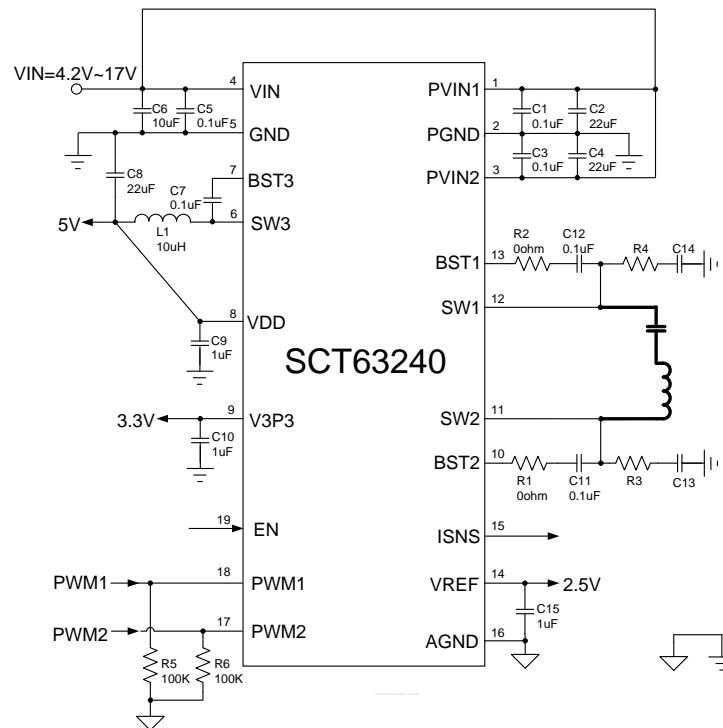# APPLICATION INFORMATION

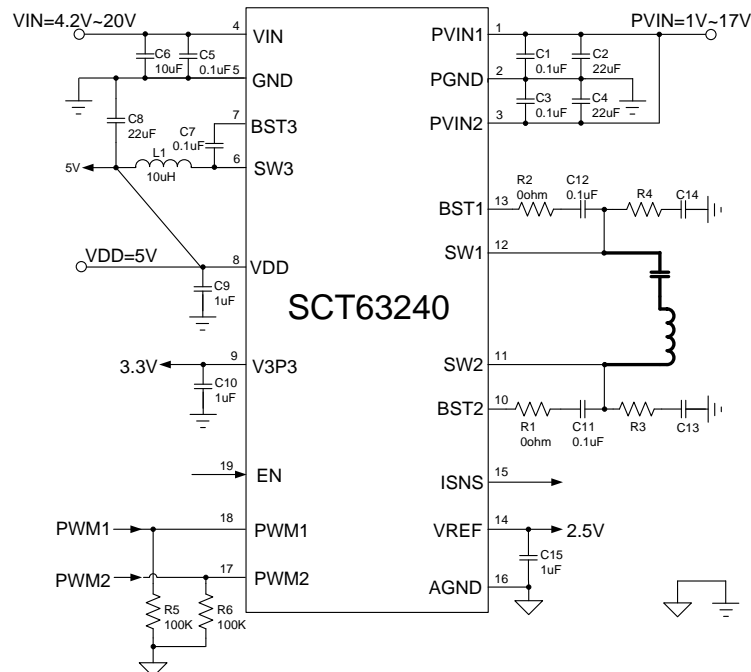**Typical Application**

Figure 10. Same Input to VIN and PVIN

Figure 11. Separate Input to VIN and PVIN

SCT63240
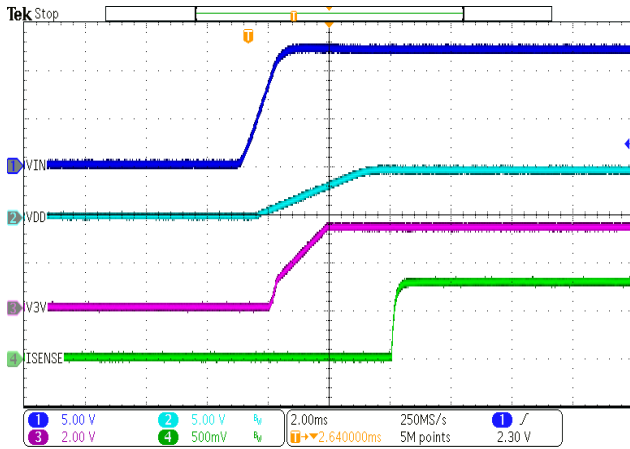
Application Waveforms

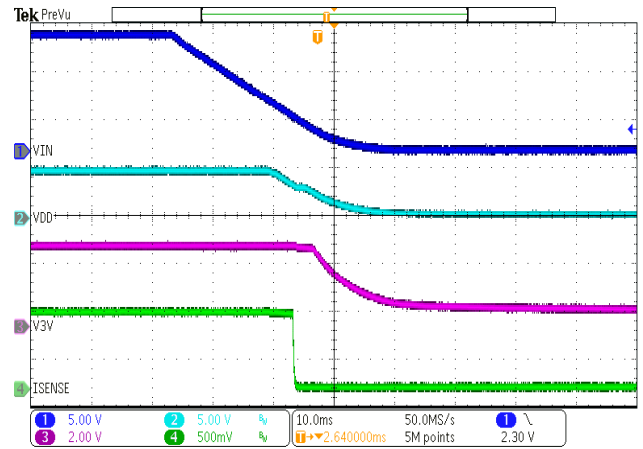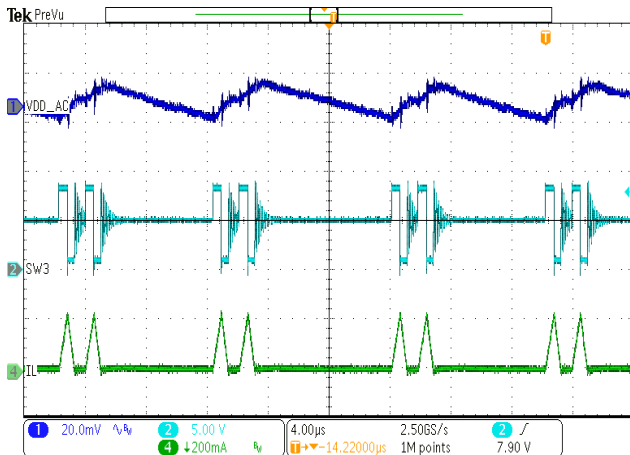

Figure 12. Power Up

Figure 13. Power Down

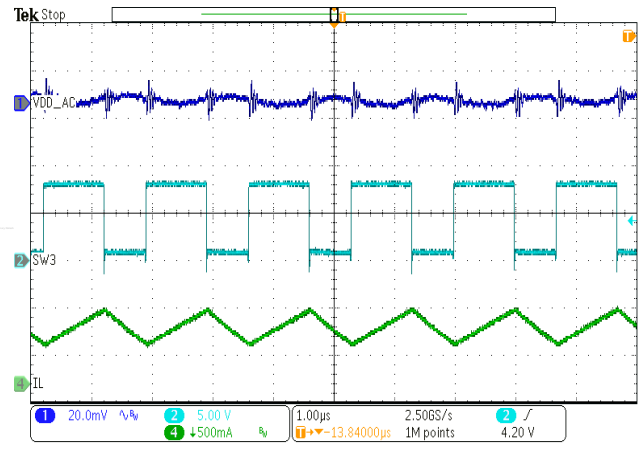Figure 14. VDD Ripple and SW3 @VIN=9V, IOUT=20mA
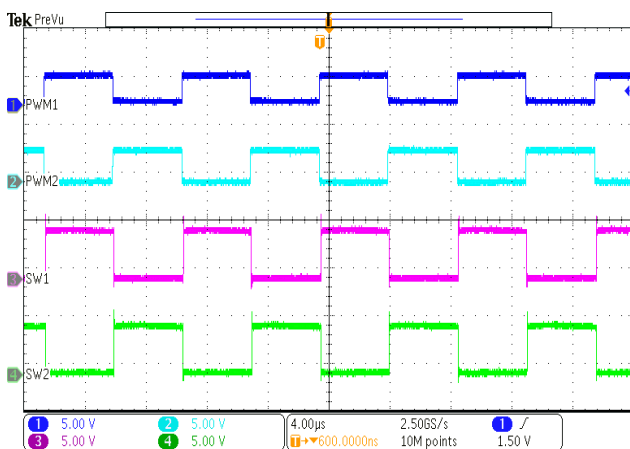

Figure 15. VDD Ripple and SW3 @VIN=9V, IOUT=600mA
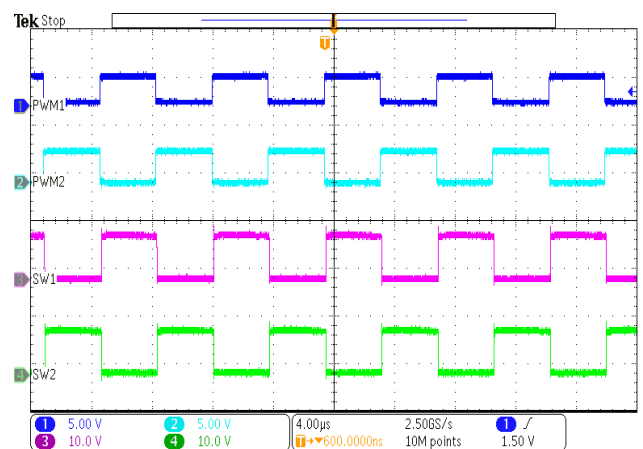

Figure 16. Full bridge @Vin=5V, RX=5W

Figure 17. Full bridge @Vin=9V, RX=10W

Layout Guideline

Proper PCB layout is a critical for SCT63240's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Buck converter output capacitor's ground should connect to GND directly to minimize the power loop.
5. VDD pin can connect to the DC/DC's output capacitor from bottom layer, connect to the point behind the capacitor while not connect to inductor.
6. Bypass capacitor for VDD place next to VDD pin.
7. Bypass capacitor for V3P3 place next to V3P3 pin.
8. Bypass capacitor for VREF place next to VREF pin.
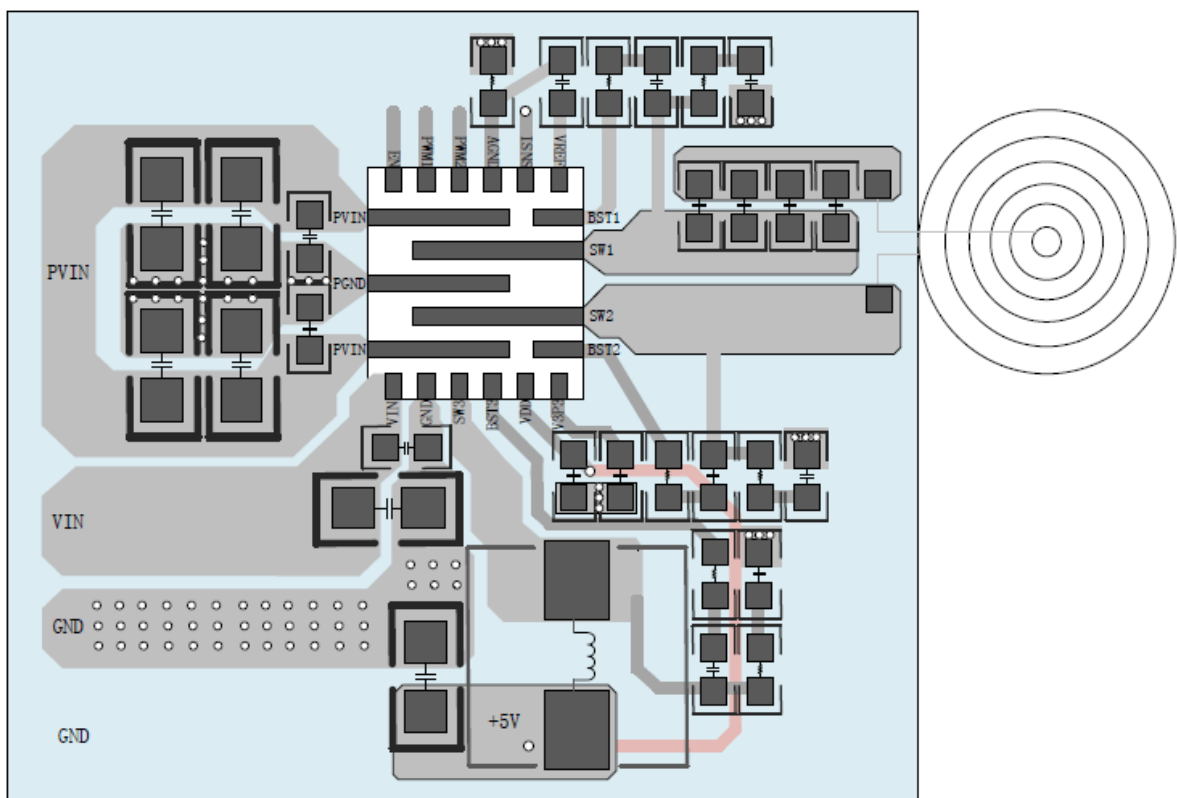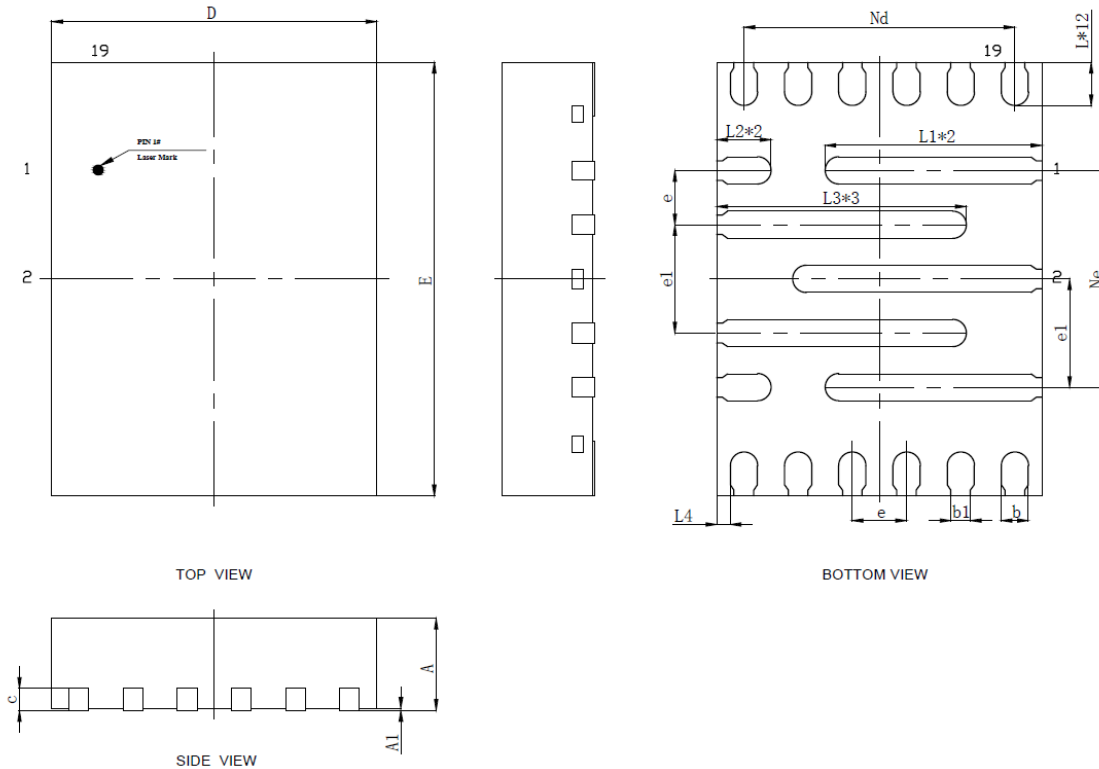9. AGND pin connect to common ground by Kelvin connection.

Figure 24. PCB Layout Example

SCT63240

PACKAGE INFORMATION

TOP VIEW

SIDE VIEW

BOTTOM VIEW

FCQFN-19L (3x4) Package Outline Dimensions

| Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c		0.203 REF	
D	2.90	3.00	3.10
Nd		2.50 BSC	
Ne		2.00 BSC	
e		0.50 BSC	
e1		1.00 BSC	
E	3.90	4.00	4.10
L	0.35	0.40	0.45
L1	1.95	2.00	2.05
L2	0.45	0.50	0.55
L3	2.25	2.30	2.35
L4	0.075	0.125	0.175

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.
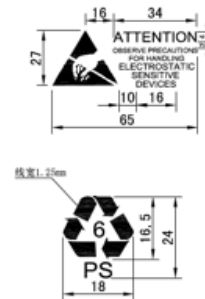
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT63240FIAR	QFN 3mmx4mm	19	5000

SCALE: 1 : 1
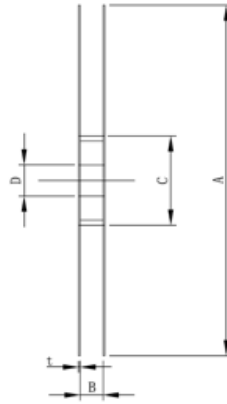
SECTION A-A

REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3
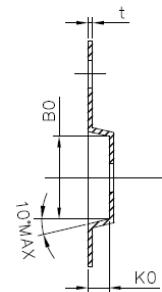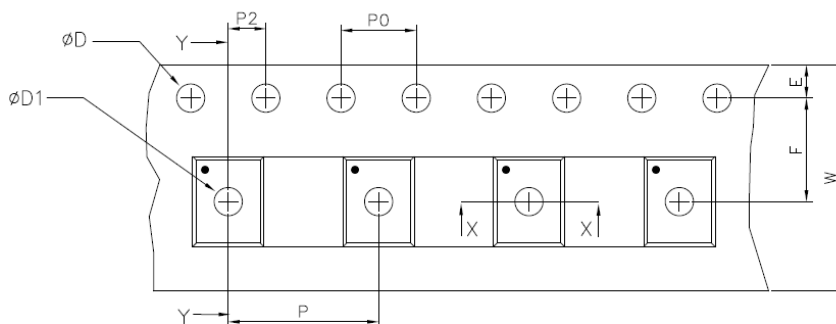
SECTION Y—Y
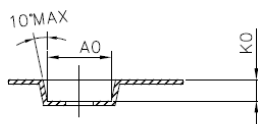
SECTION X—X

TAPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
$12^{+0.30}_{-0.10}$	3.40±0.10	4.40±0.10	1.14±0.10	0.25±0.02	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.05	2.00±0.05	$1.50^{+0.10}_{0}$	$1.50^{+0.25}_{0}$	4.00±0.10	40.0±0.20