120V Supply, 4A Peak, High Frequency High-Side and Low-Side Gate Driver

FEATURES

- Wide supply rail from 8V-24V
- Drives Both High-side and Low-side N-Channel MOSFET
- 4A Peak Output Source and Sink Current
- Bootstrap Supply Voltage Range up to 120V
- Integrated Bootstrap Diode
- TTL Compatible Input, -10V Input Capability
- Quiescent Current 252uA
- 45ns Propagation Delay Times
- 2ns Delay Matching
- 7ns Rise and 4.5ns Fall Time with 1000pF Load
- 15ns Input Deglitching Time
- 40ns Minimum Pulse Width
- Supply Rail Under-Voltage Lockout (UVLO)
- Operation from -40°C~150°C
- Available in SOP-8L, ESOP-8L, DFN-9L 3mm x 3mm, DFN-10L 3mm x 3mm and DFN-8L 4mm x 4mm Package

DESCRIPTION

The SCT52A40 is a wide supply, high frequency gate drivers including both high side and low side drivers, which are used in half-bridge, full-bridge, and buck converter to drive the discrete N-Type MOSFETs. 4A Peak Source and Sink current capability increase the power converter power efficiency.

The SCT52A40 features wide input hysteresis that is compatible for TTL low voltage logic. The SCT52A40 has the capability to handle negative input down to -10V, which increases the input noise immunity. The ability to withstand maximum of -18V on HS pin largely extend the SCT52A40 application flexibility to handle the switching node noise.

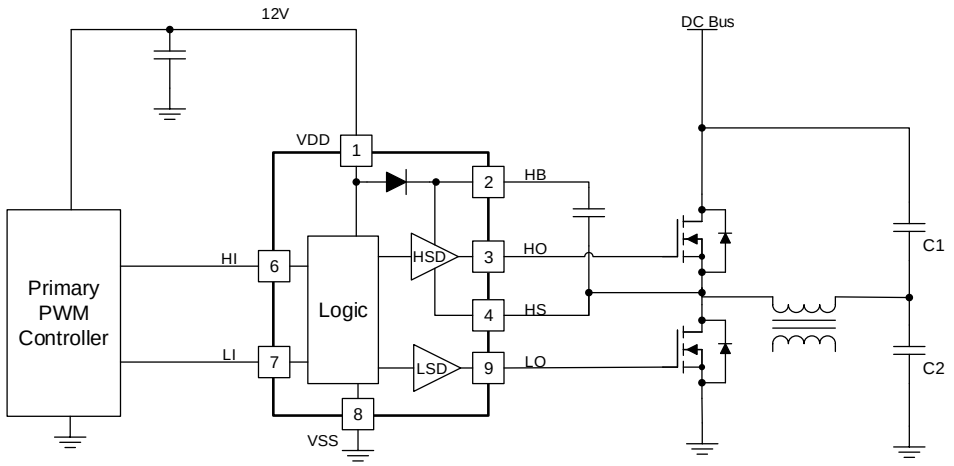
The 40ns minimum pulse width enables the SCT52A40 suitable for high frequency power converter application.

The SCT52A40 is available in DFN-9L 3mm x 3mm, DFN-8L 4mm x 4mm, ESOP-8L and SOP-8L package.

APPLICATIONS

- Battery Powered Hand Tool
- Solid-State Motor Drives
- Half-Bridge and Full-Bridge Power Converter
- Two Switch Forward Power Converters
- Active-Clamp Forward Converters

TYPICAL APPLICATION



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Add SCT52A40DRA.

Revision 1.2: Add HS pulse voltage spec in ABS max rating table.

Revision 1.3: Add limit values for T_{MON} and T_{MOFF} in ELECTRICAL CHARACTERISTICS.

Revision 1.4: Update package information

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52A40DRAR	Tape & Reel	5000	2A40	10	DFN-10L
SCT52A40DSAR	Tape & Reel	5000	2A40	9	DFN-9L
SCT52A40DTCR	Tape & Reel	5000	2A40	8	DFN-8L
SCT52A40STER	Tape & Reel	4000	2A40	8	ESOP-8L
SCT52A40STDR	Tape & Reel	4000	2A40	8	SOP-8L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VDD	-0.3	26	V
HI, LI	-10	26	V
LO (DC)	-0.3	V_{DD} + 0.3	V
LO (Pulse < 100ns) (3)	-2	V_{DD} + 0.3	V
HB	-0.3	120	V
HB-HS	-0.3	26	V
HO (DC)	V_{HS} - 0.3	V_{HB} + 0.3	V
HO (Pulse < 100ns) (3)	V_{HS} - 2	V_{HB} + 0.3	V
HS (DC)	-1	120	V
HS (Pulse < 300ns) (3)	-3	120	V
HS (Pulse < 100ns) (3)	-18	120	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

(3) Values are verified by characterization and are not production tested.

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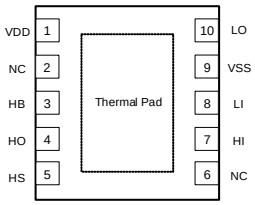
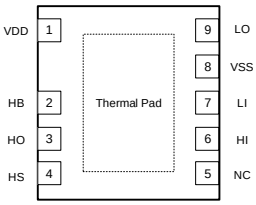
PIN CONFIGURATION

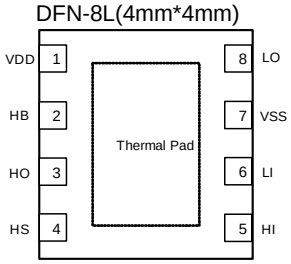
Top View
DFN-10L(3mm*3mm)



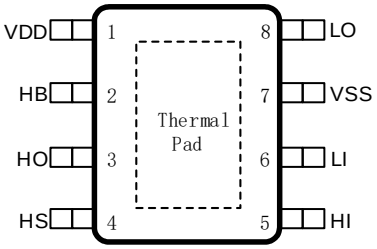
Top View
DFN-9L(3mm*3mm)



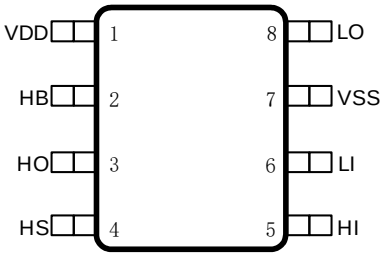
Top View
DFN-8L(4mm*4mm)



Top View
ESOP-8L



Top View
SOP-8L



PIN FUNCTIONS

NAME	DFN-10L	DFN-9L	DFN-8L	ESOP-8L	SOP-8L	PIN FUNCTION
	NO.	NO.	NO.	NO.	NO.	
VDD	1	1	1	1	1	Power Supply, must be locally bypassed by the ceramic cap.
NC	2	N/A	N/A	N/A	N/A	Not Connected.
HB	3	2	2	2	2	Bootstrap power supply for high side driver. A ceramic cap connected between HB and HS, typical value is 0.1uF.
HO	4	3	3	3	3	High side driver output.
HS	5	4	4	4	4	Switching Node, high side MOSFET source.
NC	6	5	N/A	N/A	N/A	Not Connected.
HI	7	6	5	5	5	High side driver logic input, TTL compatible. Floating logic low.
LI	8	7	6	6	6	Low side driver logic input, TTL compatible. Floating logic low.
VSS	9	8	7	7	7	Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact.
LO	10	9	8	8	8	Low side driver output

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	8	24	V
$V_{HI,LI}$	Driver input voltage range	-10	24	V
V_{HS}	Voltage on HS	-1	120	V
	Slew rate on HS		50	V/ns
V_{HB}	Voltage on HB	V_{HS}+8	120	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-10L 3x3mm	DFN-9L 3x3mm	DFN-8L 4x4mm	ESOP-8L	SOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	43.7	43.7	36.2	40.5	106.5	°C/W
$R_{\theta JC}$	Junction to case thermal resistance (1)	49.9	49.9	41.6	49	52.9	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT52A40 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT52A40. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Currents						
I_{DD}	VDD quiescent current	VHI=VLI=0		252		uA
I_{VDDO}	VDD operating current	Fsw=500kHz, CLoad=0nF		2.27		mA
I_{HB}	HB quiescent current	VHI=VLI=0		168		uA
I_{HBO}	HB operating current	Fsw=500kHz, CLoad=0nF		2		mA
I_{HBS}	HB to VSS quiescent current	VHS=VHB=110V			1	uA
I_{HBSO}	HB to VSS operating current	Fsw=500kHz, CLoad=0nF		1.1		mA
INPUTS						
$V_{HI, LI}$	Input logic high threshold			2.1	2.4	V
	Input logic low threshold		0.8	1		V
V_{HI, LI_Hys}	Hysteresis			1.1		V
	Input pull down resistance			200		KΩ
UNDERVOLTAGE PROTECTION(UVLO)						
V_{DDR}	VDD rising threshold			7.18		V
V_{DDHYS}	VDD threshold hysteresis			0.63		V
V_{HBR}	HB rising threshold			6.7		V
V_{HBHYS}	HB threshold hysteresis			0.43		V
LO GATE DRIVER						
V_{LOH}	Output high voltage	I_{OUT}= - 10mA, $V_{LOH}=V_{DD}-V_{LO}$			10	mV
V_{LOL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF		4		A
R_{LOH}	Output pull high resistance	I_{OUT}= - 10mA		1		Ω
R_{LOL}	Output pull low resistance	I_{OUT}= 10mA		0.7		Ω
HO GATE DRIVER						
V_{HOH}	Output high voltage	I_{OUT}= - 10mA, $V_{HOH}=V_{HB}-V_{HO}$			10	mV
V_{HOL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF		4		A
R_{HOH}	Output pull high resistance	I_{OUT}= - 10mA		1		Ω
R_{HOL}	Output pull low resistance	I_{OUT}= 10mA		0.7		Ω
BOOTSTRAPE DIODE						
VFL	Low current forward voltage	IVDD - HB=100uA		0.64		V
VFH	High current forward voltage	IVDD – HB=100mA		0.88		V
RD	Dynamic resistance			0.7		Ω
OUTPUT RISE AND FALL TIME						
T_{R_LO}	Low side driver output rising time	C_{Load}=1nF		7		ns
T_{F_LO}	Low side driver output falling time	C_{Load}=1nF		4.5		ns
T_{R_HO}	High side driver output rising time	C_{Load}=1nF		7		ns
T_{F_HO}	High side driver output falling time	C_{Load}=1nF		4.5		ns
T_{R_LO}	Low side driver output rising time	C_{Load}=100nF		0.4		us

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{F_LO}	Low side driver output falling time	C_{Load}=100nF		0.33		us
T_{R_HO}	High side driver output rising time	C_{Load}=100nF		0.4		us
T_{F_HO}	High side driver output falling time	C_{Load}=100nF		0.33		us
PROPAGATION DELAYS						
T_{DRL}	LI to LO propagation delay, Rising edge	C_{Load}=0nF		46		ns
T_{DFL}	LI to LO propagation delay, Falling edge	C_{Load}=0nF		45		ns
T_{DRH}	HI to HO propagation delay, Rising edge	C_{Load}=0nF		46		ns
T_{DFH}	HI to HO propagation delay, Falling edge	C_{Load}=0nF		45		ns
DELAY MATCHING						
T_{MON}	HO OFF to LO ON		0	2	7	ns
T_{MOFF}	LO OFF to HO ON		0	2	12	ns
MISCELLANEOUS						
T_{MIN_ON}	Minimum input pulse width			40		ns
$T_{IN\_Deglitch}$	Input deglitch time			15		ns
T_{BST}	Bootstrap turn off time	IF=20mA, IR=0.2A		90		ns

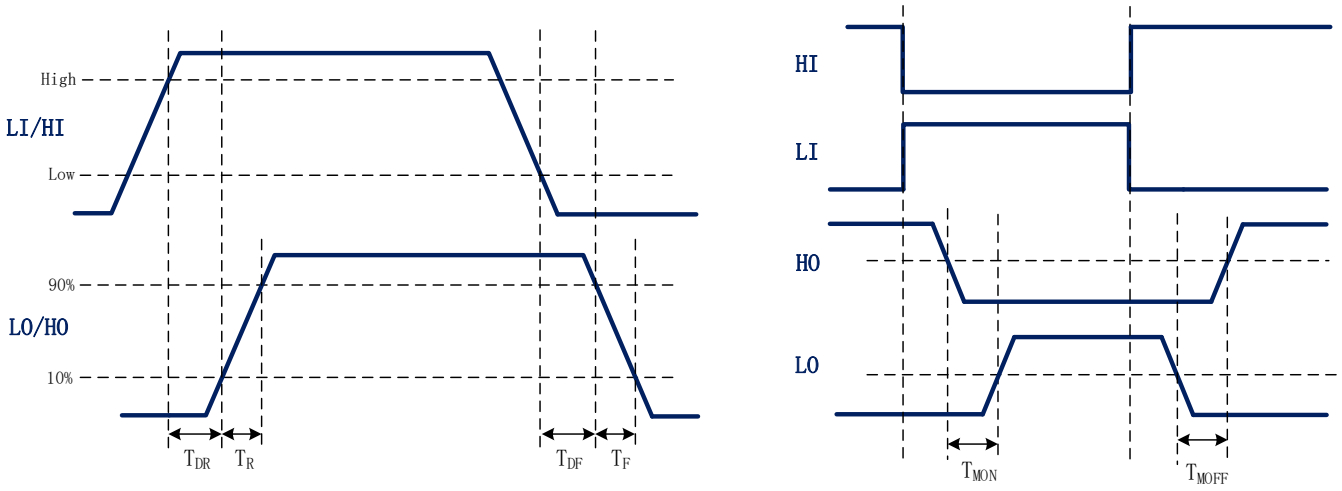

Figure 1. Timing Diagram

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TYPICAL CHARACTERISTICS

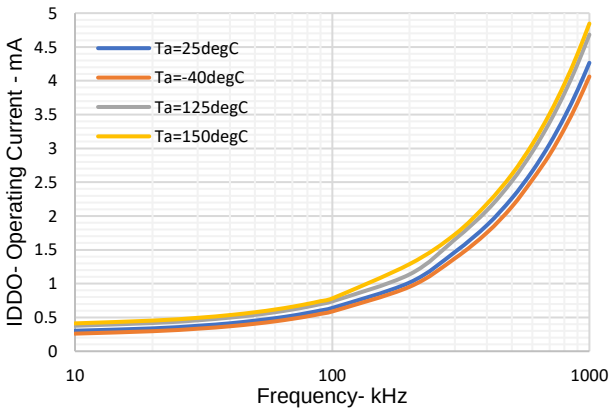

Figure 2. IDD Operating Current vs Frequency

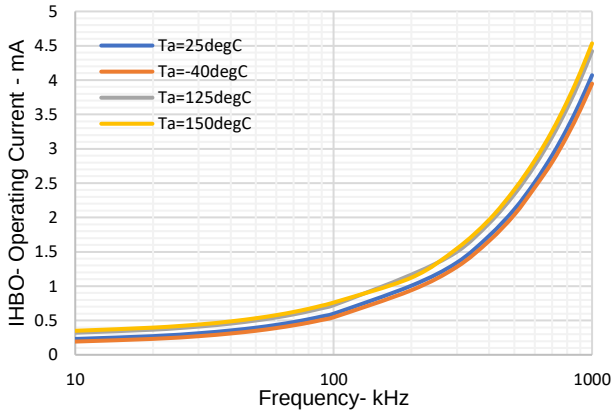

Figure 3. Boot Voltage Operating Current vs Frequency

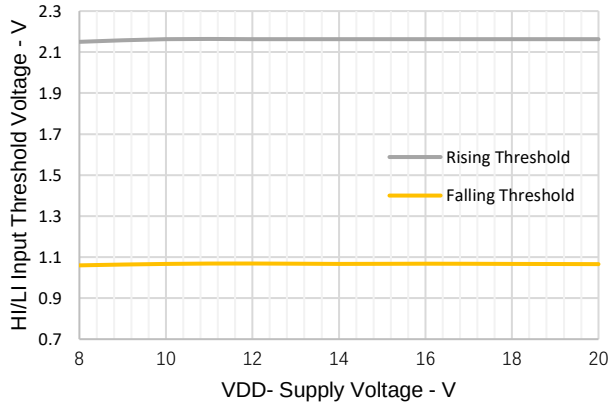

Figure 4. Input Threshold vs Supply Voltage

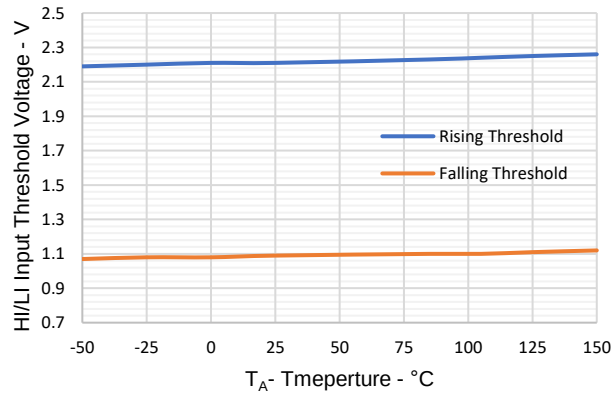

Figure 5. Input Threshold vs Temperature

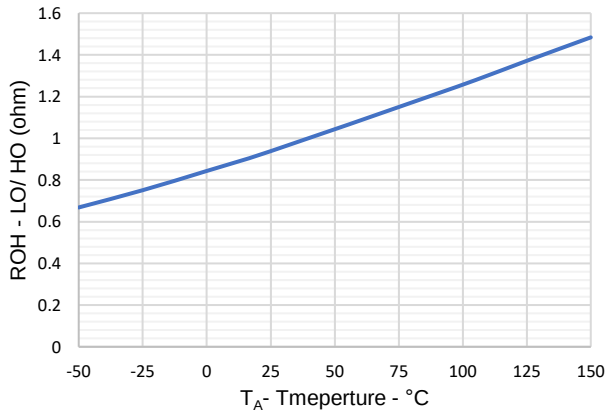

Figure 6. Output pull high resistance vs Temp

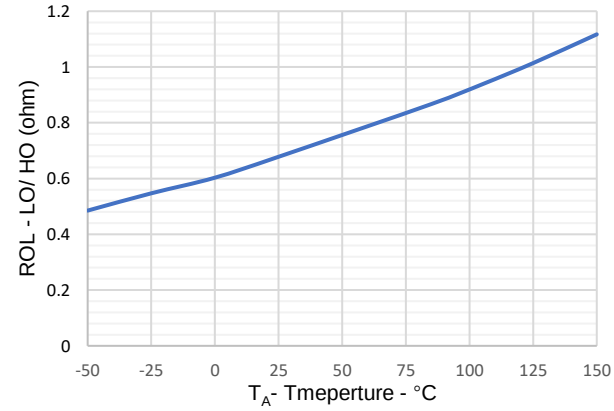

Figure 7. Output pull low resistance vs Temp

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TYPICAL CHARACTERISTICS(CONTINUED)

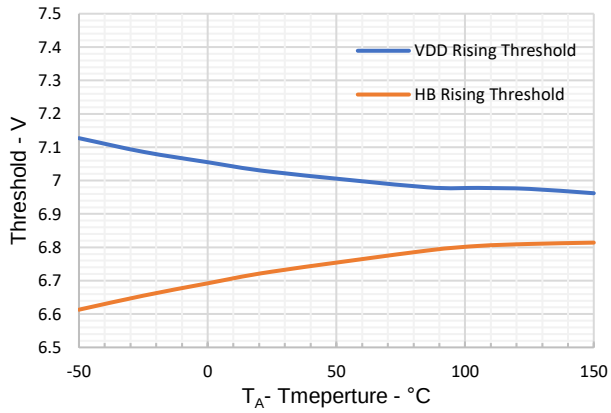

Figure 8. UVLO Threshold vs Temperature

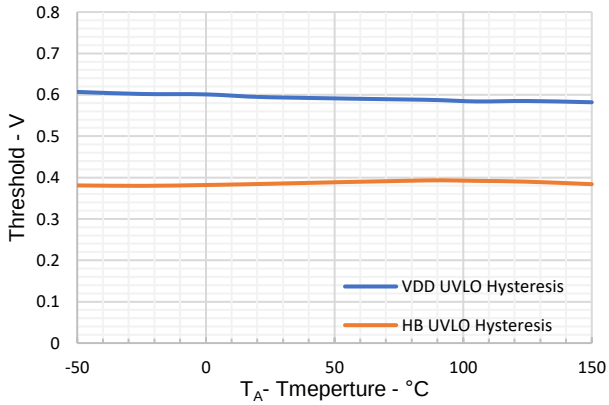

Figure 9. UVLO Threshold Hysteresis vs Temperature

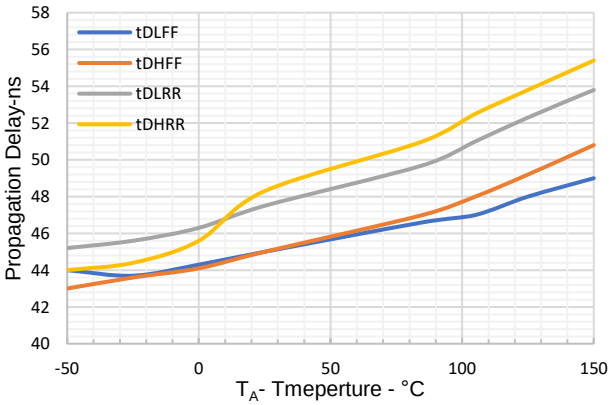

Figure 10. Propagation Delays vs Temperature

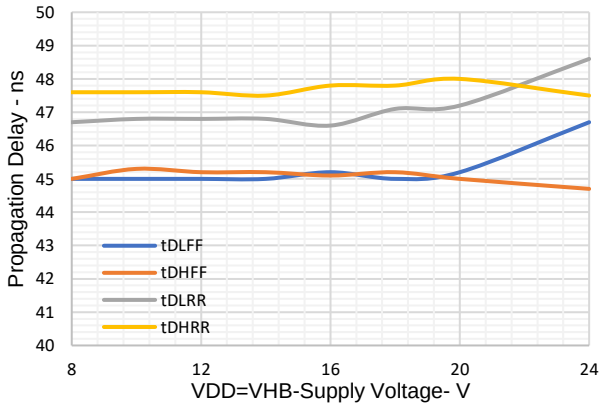

Figure 11. Propagation Delay vs Supply Voltage

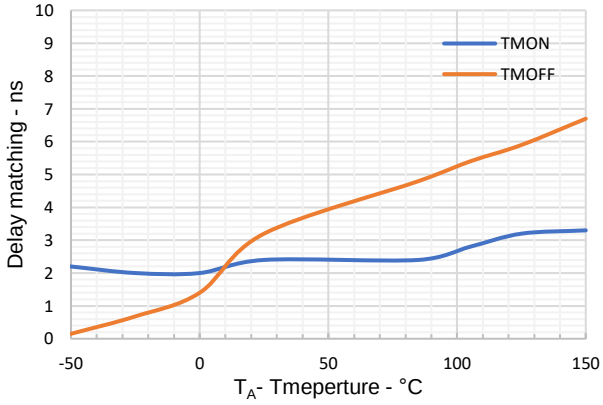

Figure 12. Delay Matching vs Temperature

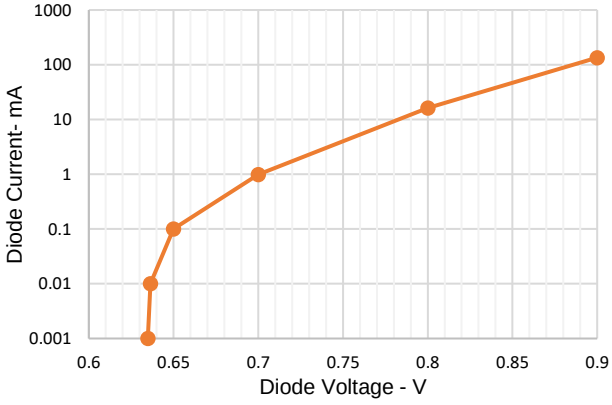

Figure 13. Diode Current vs Diode Voltage

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FUNCTIONAL BLOCK DIAGRAM

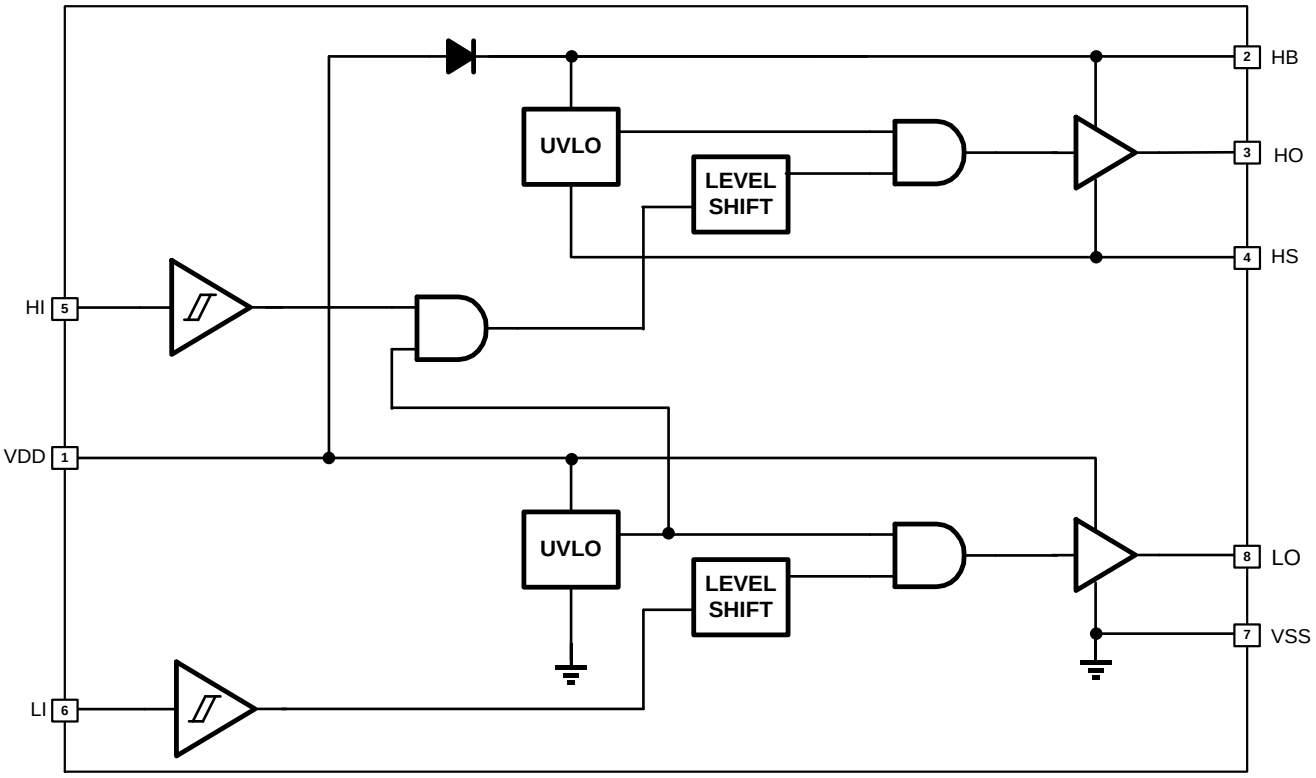

Figure 14. Functional Block Diagram

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OPERATION

Overview

The SCT52A40 is high-side and low-side drivers. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the SCT52A40. The Input of SCT52A40 is the TTL logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

Table 1: the SCT52A40 Device Logic.

HI	LI	HO	LO
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

VDD Power Supply

The SCT52A40 operates under a supply voltage range between 8V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1μF surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT52A40. In addition, a larger capacitor (such as 1μF or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Under Voltage Lockout (UVLO)

SCT52A40 device Under Voltage Lock Out (UVLO) rising threshold is typically 7.18V with 630mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise from the power supply. For example, at power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD until steady state VDD reached.

Input Stage

The input of SCT52A40 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. SCT52A40 also features tight control of the input pin threshold voltage that ensures stable operation across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

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APPLICATION INFORMATION

Typical Application

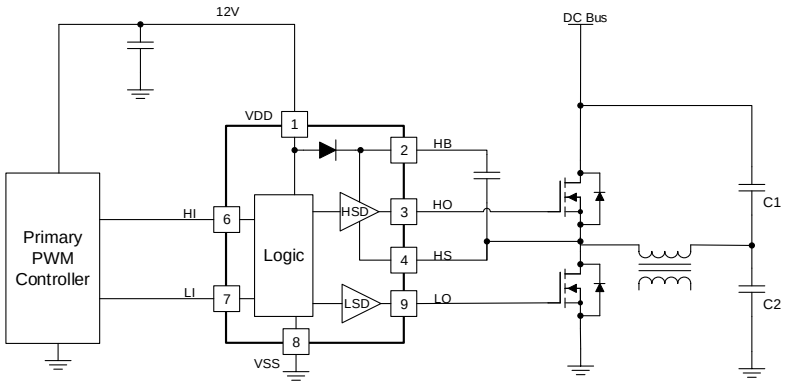

Figure 15. Dual Channel Driver Typical Application (DFN-9)

Driver Power Dissipation

Generally, the power dissipated in the SCT52A40 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52A40 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52A40 is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \quad (1)$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52A40 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \quad (2)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G}\right) \quad (3)$$

Where

- R_{OH} is the equivalent pull up resistance of SCT52A40
- R_{OL} is the pull down resistance of SCT52A40
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

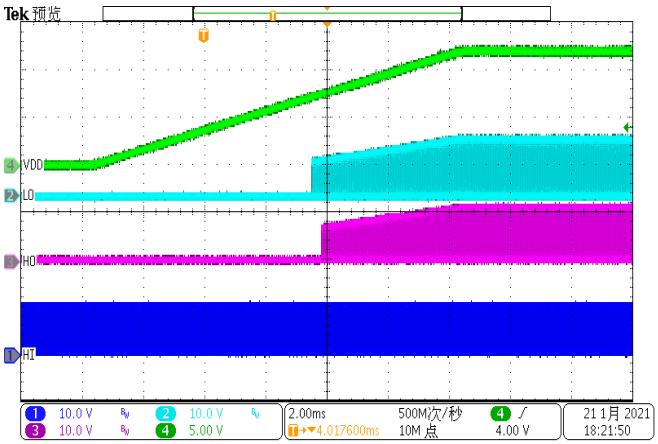

Figure 16. Power Up

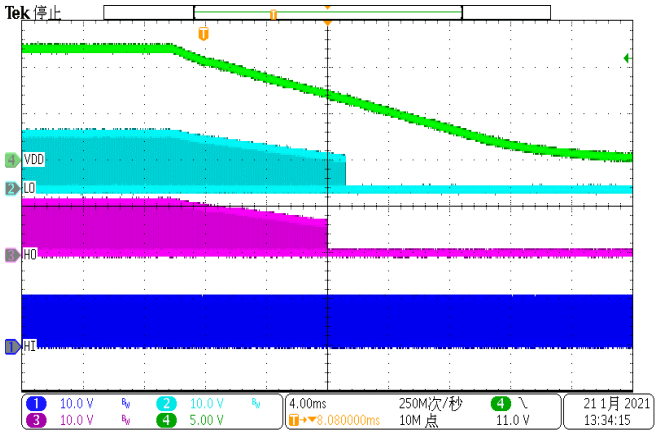

Figure 17. Power Down

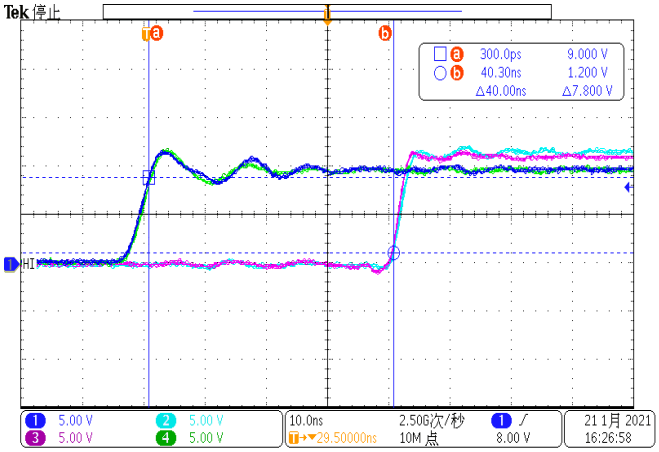

Figure 18. LO HO Rising Edge Propagation Delay, C_L=0nF

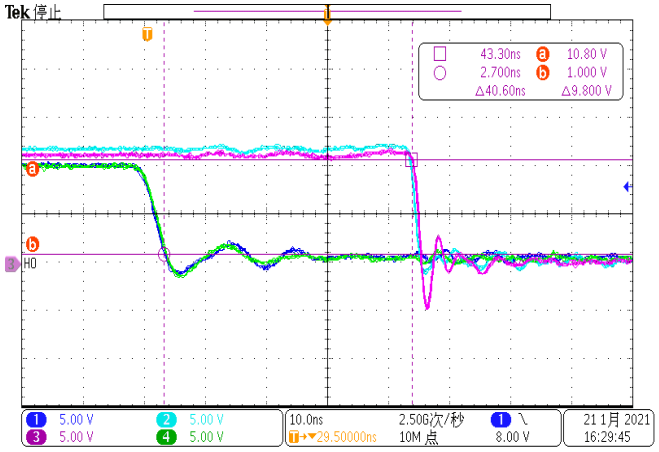

Figure 19. LO HO Falling Edge Propagation Delay, C_L=0nF

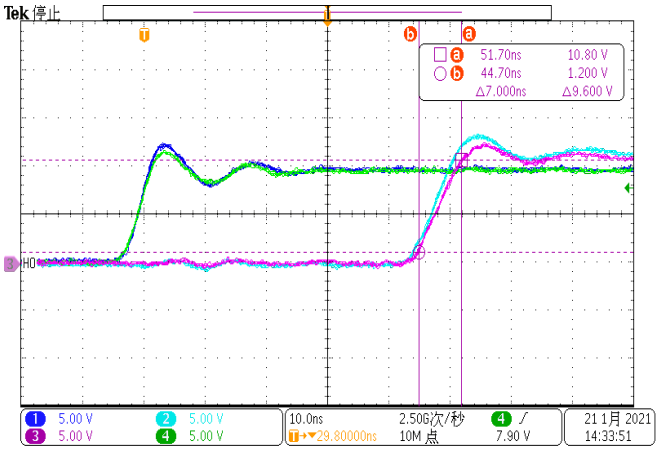

Figure 20. LO HO Rising Time, CL=1nF

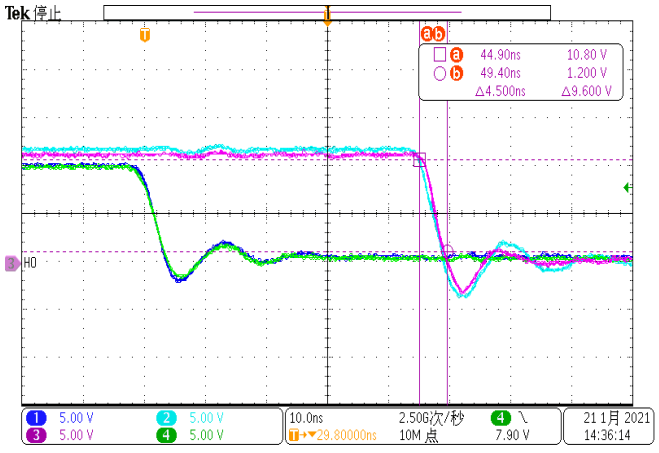

Figure 21. LO HO Falling Time, CL=1nF

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Layout Guideline

The SCT52A40 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

1. Put the SCT52A40 as close as possible to the power devices to minimize the gate driving loop including the driver output and power device gate.
2. Locate the VDD and VHB (bootstrap) capacitors as close as possible to the driver to reduce the supply ripple.
3. Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from SCT524A40 does directly to the source of the low-side MOSFET, but not be in the high current path of MOSFET source current.
4. Use the same rules for HS as for GND for the high-side MOSFET.
5. Use wide trace for LO and HO to decrease the influence of switching ringing made by parasitic inductance.
6. Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another.
7. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
8. Avoid LI and HI (driver input) going close to the HS node or any other high dv/dt traces that can induce significant noise into the relatively high impedance leads.
9. For the output stackable application, the driver input loop of two-channel input must be strictly symmetrical to ensure the input propagation delay is the same.
10. Star-point grounding is recommending to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane is to provide noise shielding and thermal dissipation as well.

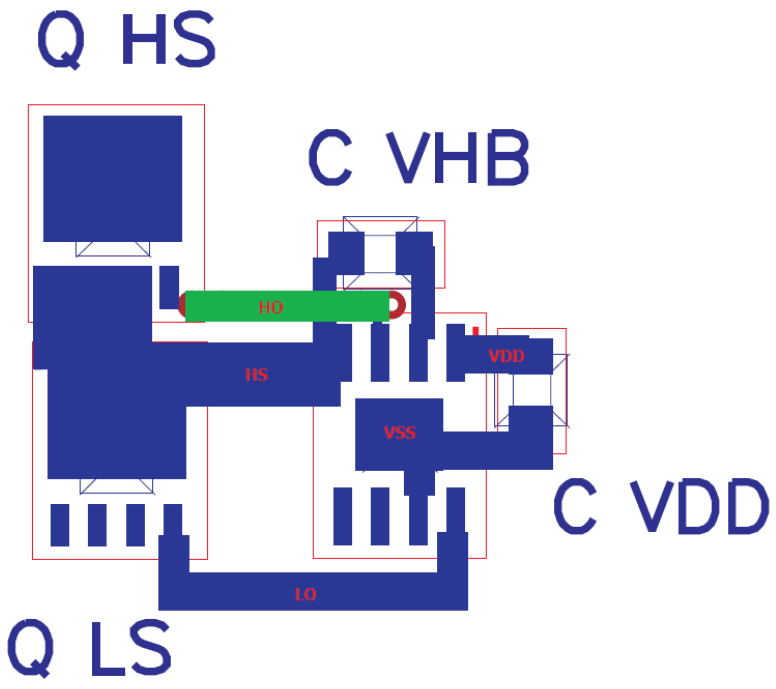

Figure 22. SCT52A40 PCB Layout Example

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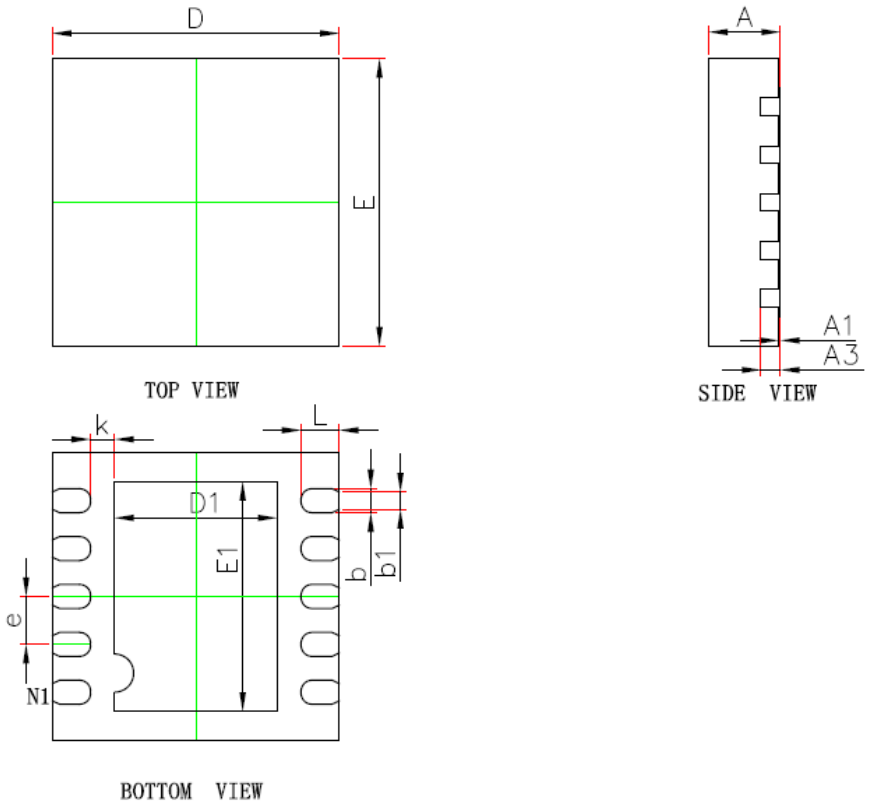
PACKAGE INFORMATION (DFN3*3-10L)



DFN3X3-10L Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
b	0.200	0.300	0.008	0.012
k	0.250 REF.		0.010 REF.	
b1	0.180 REF.		0.007 REF.	
e	0.500 BSC.		0.020 BSC.	
L	0.324	0.476	0.013	0.019

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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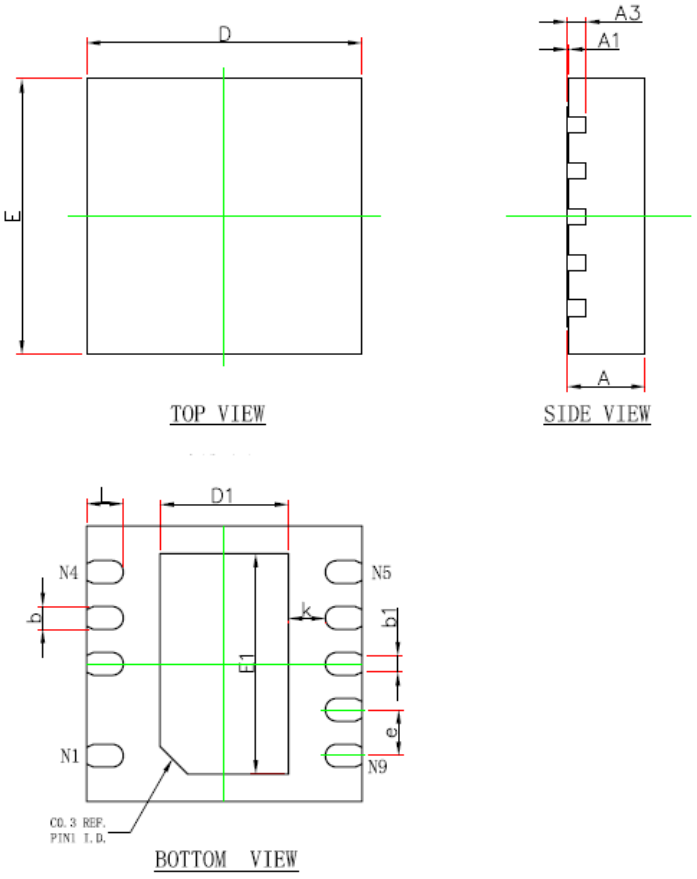
PACKAGE INFORMATION (DFN3*3-9L)



DFN3X3-9L Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.800	0.900	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.300	1.500	0.051	0.059
E1	2.300	2.500	0.091	0.098
k	0.400 REF.		0.016 REF.	
b	0.200	0.300	0.008	0.012
b1	0.180 REF.		0.007 REF.	
e	0.500 BSC.		0.020 BSC.	
L	0.300	0.500	0.012	0.020

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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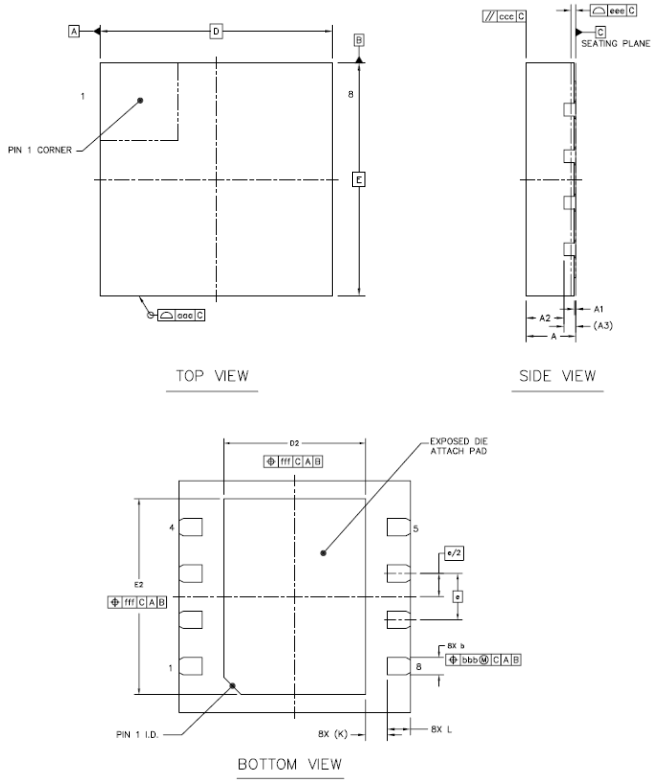
PACKAGE INFORMATION (DFN4*4-8L)



DFN4X4-8L Package Outline Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.25	0.3	0.35
D	3.9	4	4.1
E	3.9	4	4.1
e		0.8 BSC	
D2	2.35	2.45	2.55
E2	3.28	3.38	3.48
L	0.3	0.4	0.5
K		0.375 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.1	
fff		0.1	

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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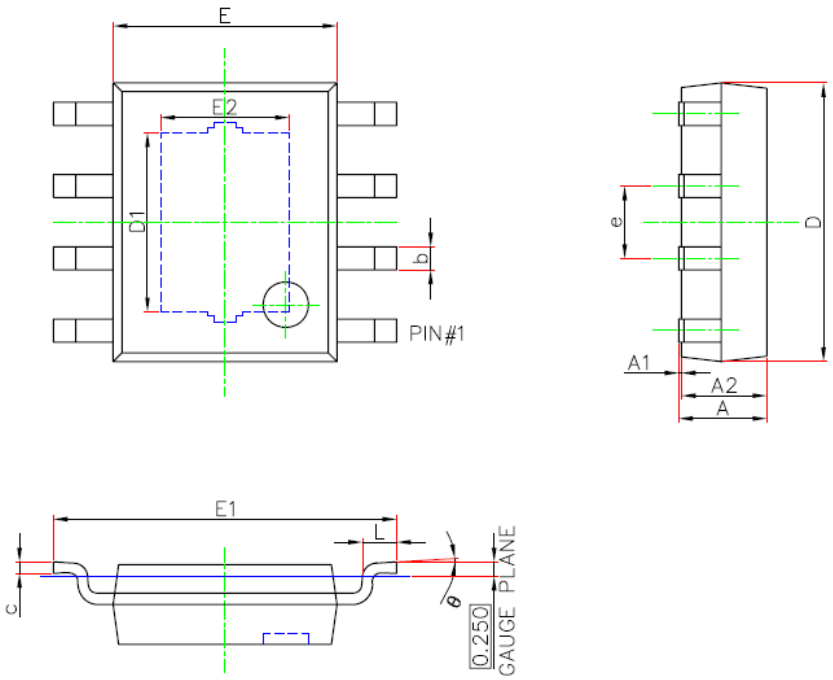
PACKAGE INFORMATION (eSOP-8)



SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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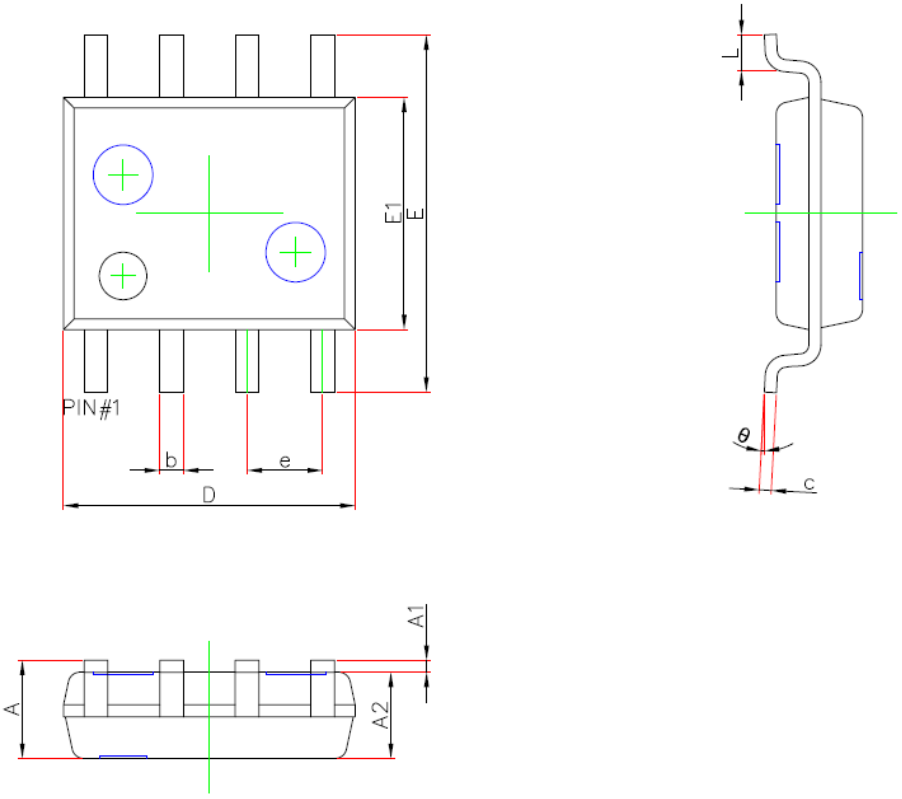
PACKAGE INFORMATION (SOP-8)



SOP8 Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
12. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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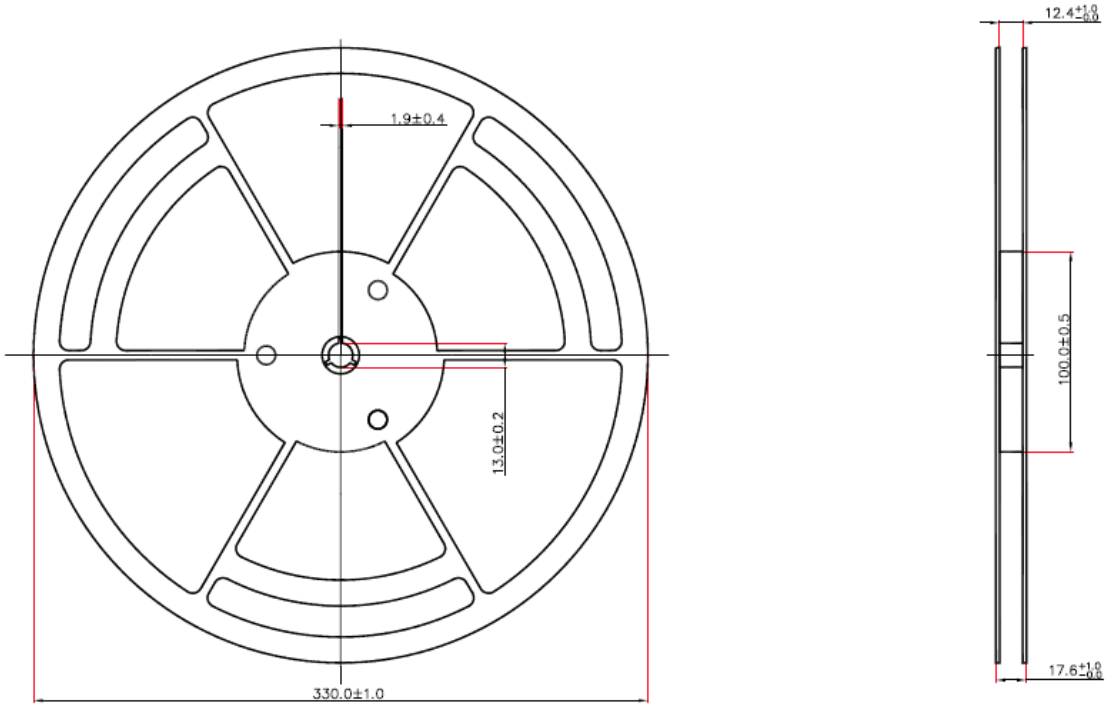
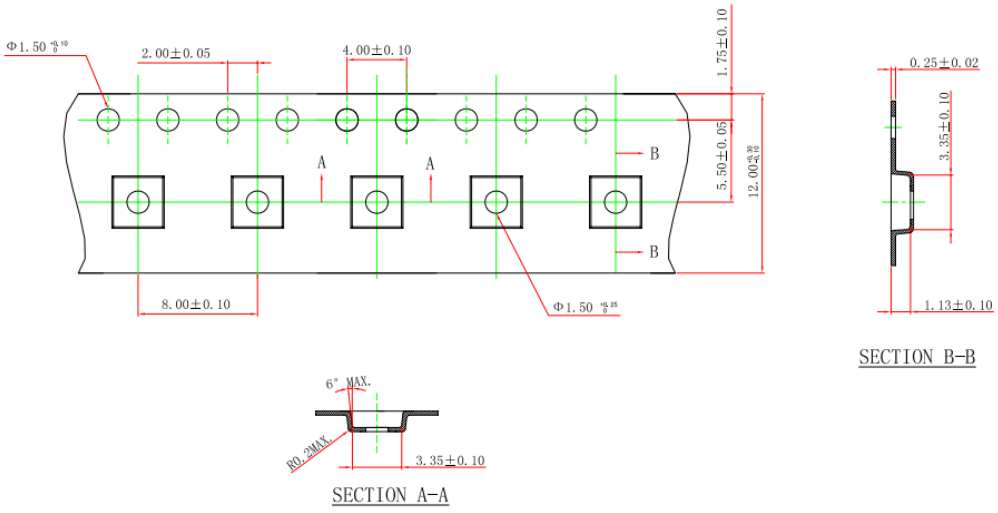
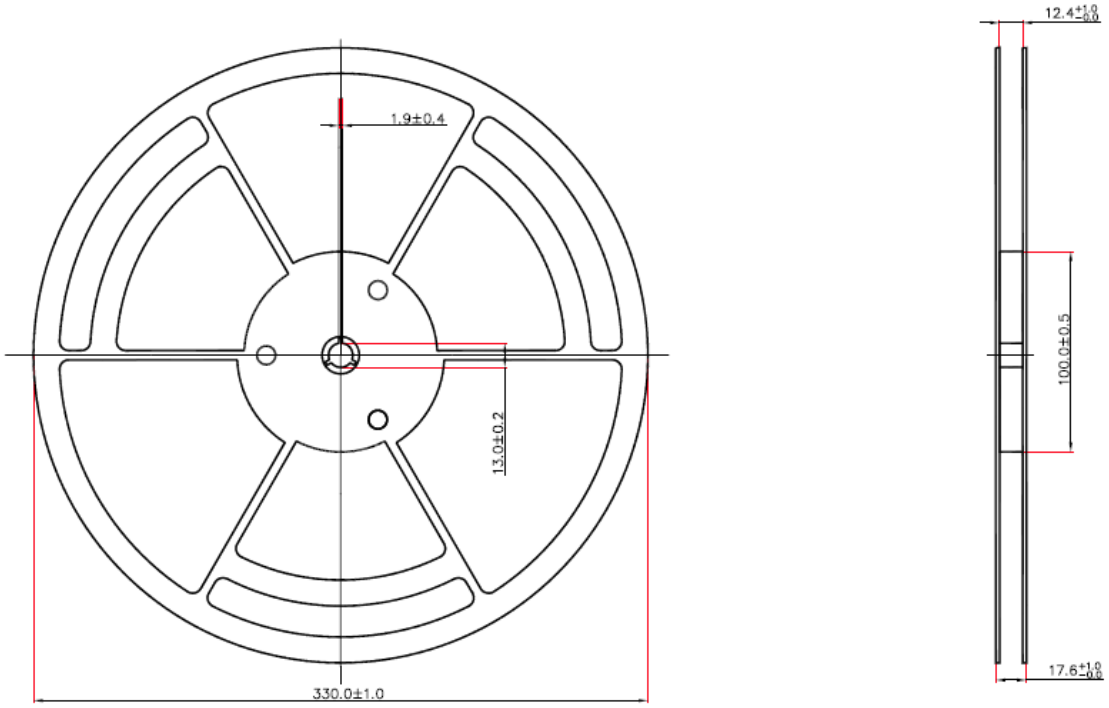
TAPE AND REEL INFORMATION(DFN-10L,DFN-9L)

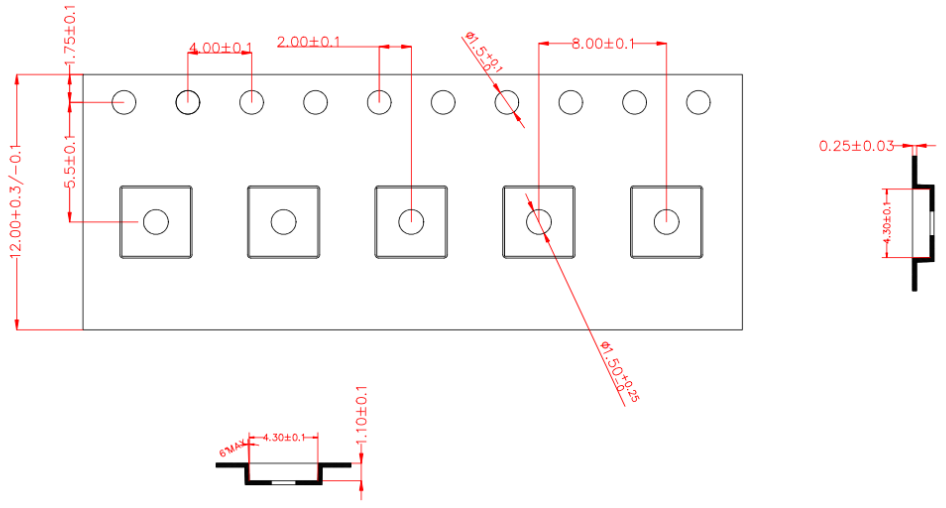




Feeding Direction

TAPE AND REEL INFORMATION (DFN-8L)





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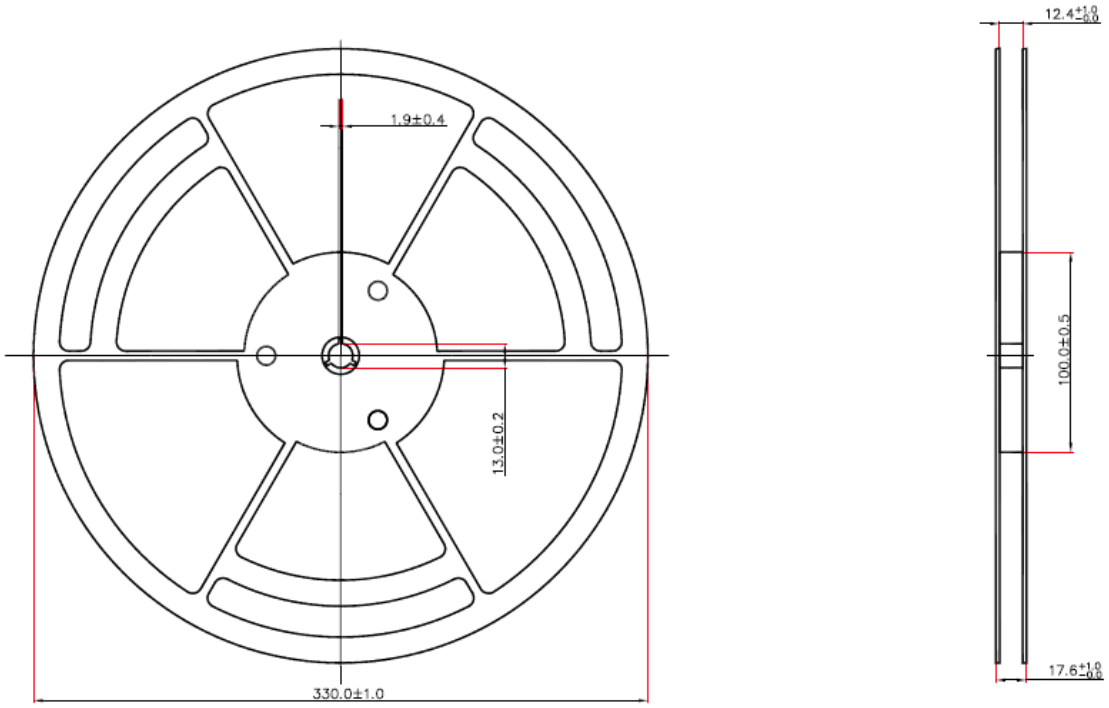
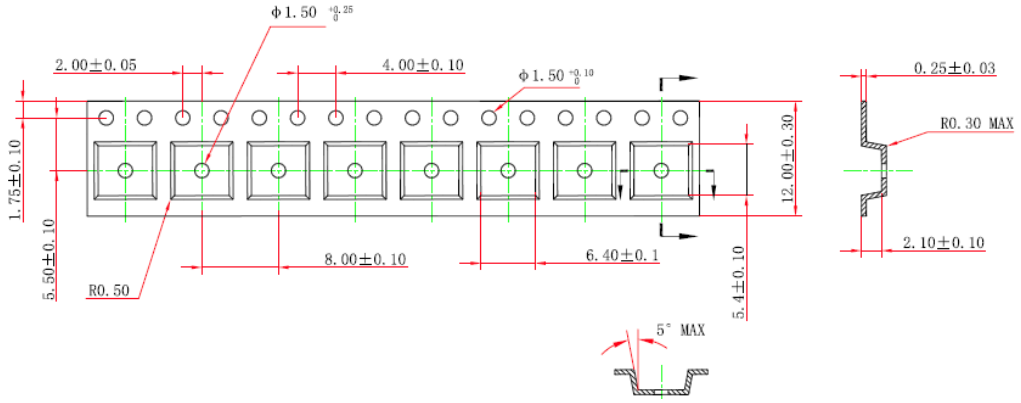
TAPE AND REEL INFORMATION (eSOP-8,SOP-8)





Feeding Direction