4.5V-40V Vin, 1A Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Range: 4.5V-40V
- Up to 1A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 600mΩ High-Side and 300mΩ Low-Side Power MOSFETs
- Fixed Frequency 1.2MHz
- Pulse Skipping Mode (PSM) at Light Load
- 90uA Quiescent Current in Sleep Mode
- 80ns Minimum On-time
- 1ms Internal Soft-start Time
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Over-voltage and Over-Temperature Protection
- Available in an TSOT23-6L Package

APPLICATIONS

- Industrial 24V Distributed Power Bus
- Power meter
- Elevator, PLC, Servo
- Automatic Control
- Automotive

DESCRIPTION

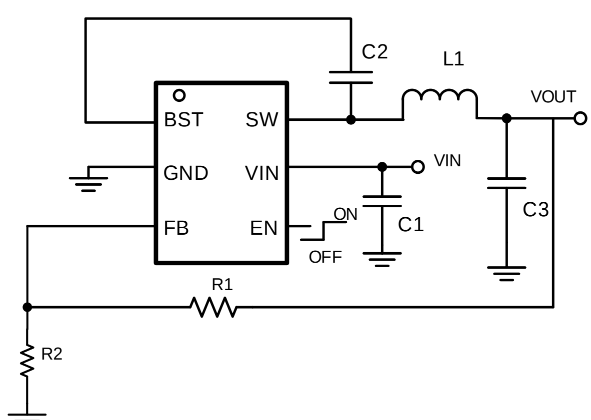
The SCT2411 is a high frequency, up to 1A continuous output synchronous buck converter. It has wide input voltage rating from 4.5V to 40V, which integrates a 600mΩ high-side MOSFET and a 300mΩ low-side MOSFET. The S4CT2411, adopts the peak current mode control with built-in loop compensation to make the chip easy to use.

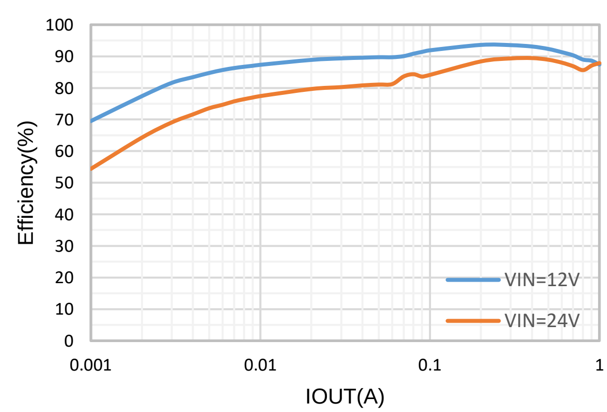
The SCT2411 features fixed 1.2MHz switching frequency, which minimizes the external off chip passive components size and reduces the output ripple to be lower than 0.1% of output when the output is 12V. With a minimum 80ns on-time of high-side MOSFET, the SCT2411 allows power conversion from high input voltage to low output voltage.

The SCT2411 supports the Pulse Skipping Modulation (PSM) with typical 90uA low quiescent current. It achieves 87% power efficiency at 10mA light load condition.

The SCT2411 offers cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in a 6-pin small profile TSOT23-6L package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2411TVB	2411	6-Lead Plastic TSOT23-6
1）For Tape & Reel, Add Suffix R (e.g. SCT2411TVBR).		

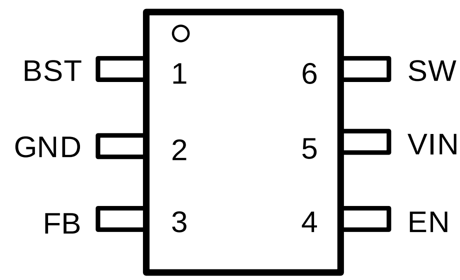
ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	42	V
BST	-0.3	48	V
SW	-1	42	V
SW（<10ns）	-2.5	48	V
BST-SW	-0.3	6	V
FB	-0.3	6	V
Operating junction temperature (2)	-40	150	C
Storage temperature T_{STG}	-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION



6-Lead Plastic TSOT23-6

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BST	1	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
GND	2	GND
FB	3	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typically.
EN	4	Enable logic input. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.21V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
VIN	5	Power supply input. Must be locally bypassed.
SW	6	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	40	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	94.18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.31	
Ψ_{JB}	Junction-to-board characterization parameter(1)	25.86	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	111.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	26.51	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2411 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2411. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.5		40	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.3 440		V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		90		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.21	1.4	V
V_{EN_L}	Enable low threshold		0.9	1.1		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			600		mΩ
R_{DSON_L}	Low side FET on-resistance			300		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		0.78	0.8	0.825	V
Current Limit						
I_{LIM_HSD}	HSD peak current limit		1.2	1.5	1.75	A
I_{LIM_LSD}	LSD valley current limit	T_J=25°C	0.8	1	1.3	A
		T_J=-40°C~125°C	0.68			A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V	960	1200	1440	kHz
t_{ON_MIN}	Minimum on-time			80		ns
Soft Start Time						
t_{SS}	Internal soft-start time			1		ms
Protection						
V_{OVP}	Feedback overvoltage with respect to	V_{FB}/V_{REF} rising		110		%
	reference voltage	V_{FB}/V_{REF} falling		105		%
T_{SD}*	Thermal shutdown threshold Hysteresis	T_J rising		170 25		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

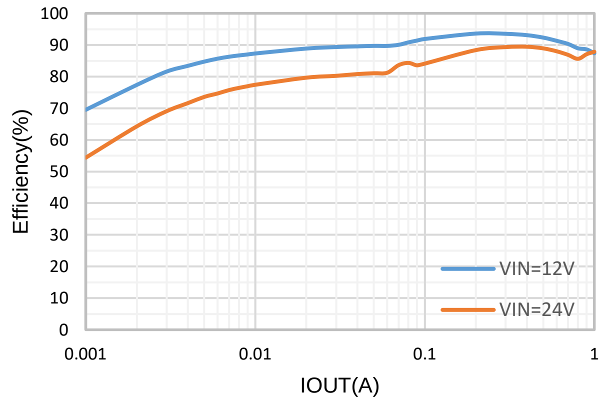


Figure 1. Efficiency vs Load Current, Vout=5V

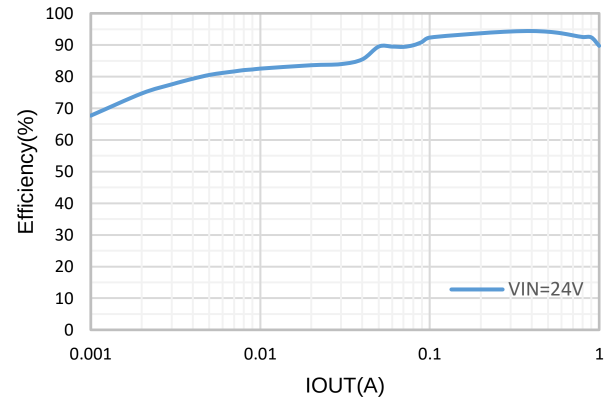


Figure 2. Efficiency vs Load Current, Vout=12V

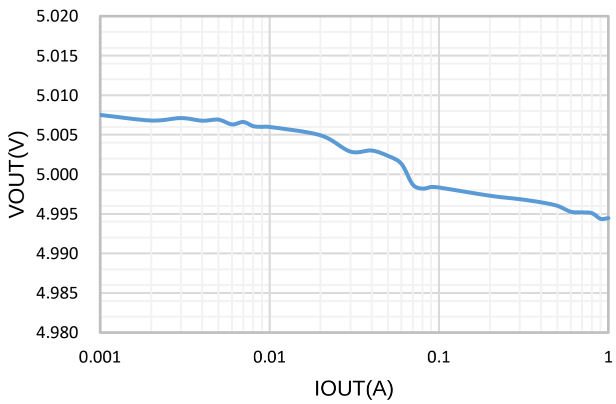


Figure 3. Load Regulation, Vout=5V, Vin=24V

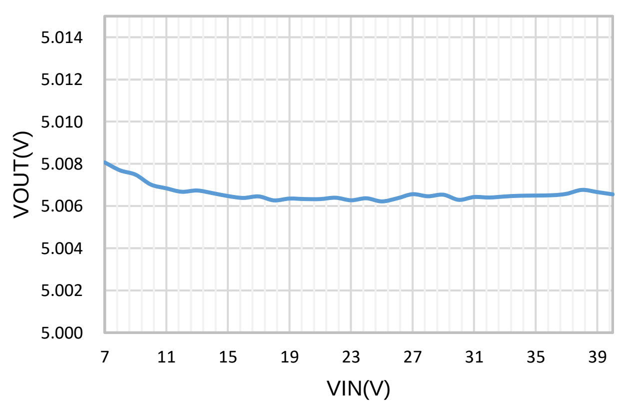


Figure 4. Line Regulation, Vout=5V, Io=0.5A

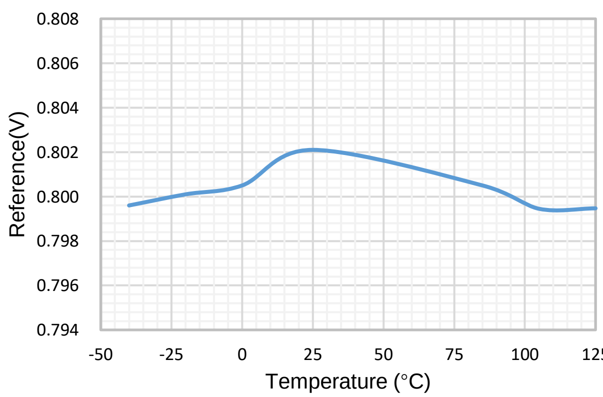


Figure 5. Reference VS Temperature

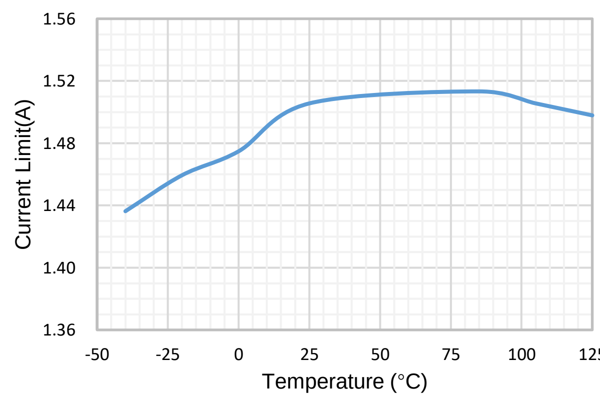


Figure 6. HS Current Limit VS Temperature

TYPICAL CHARACTERISTICS

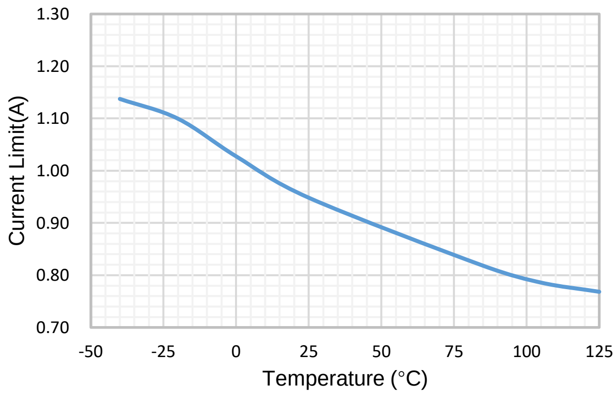


Figure 7. LS Current Limit VS Temperature

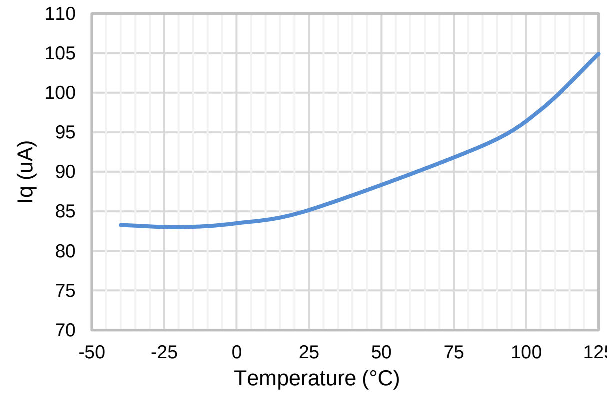


Figure 8. Quiescent Current vs Temperature Vin=12V

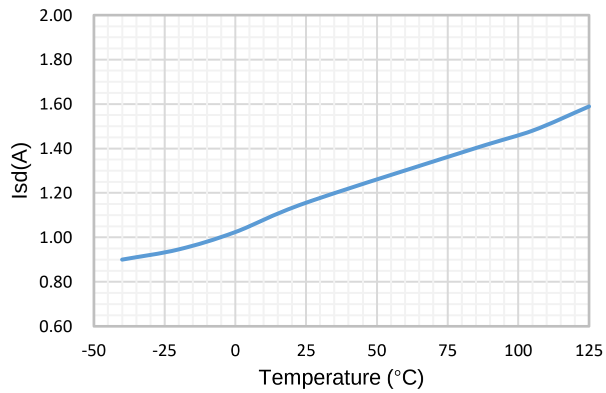


Figure 9. Shutdown Current vs Temperature, Vin=12V

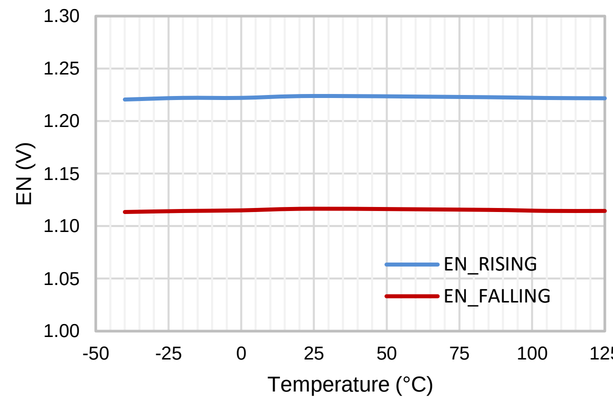


Figure 10. EN Threshold vs Temperature

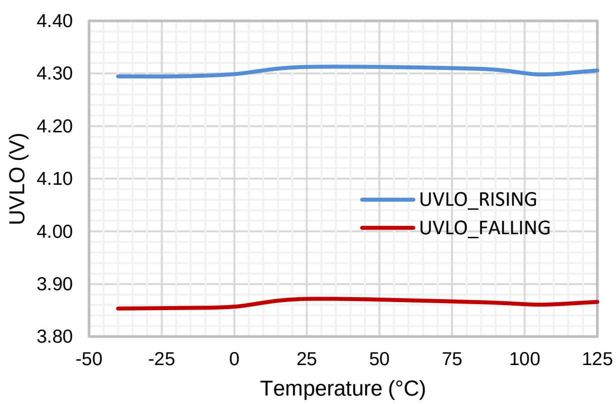


Figure 11. VIN UVLO VS Temperature

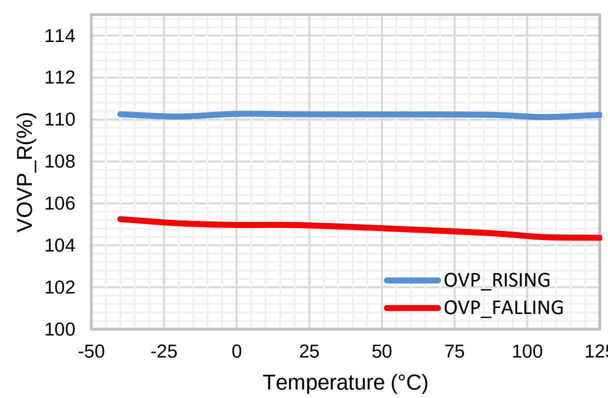


Figure 12. OVP VS Temperature

FUNCTIONAL BLOCK DIAGRAM

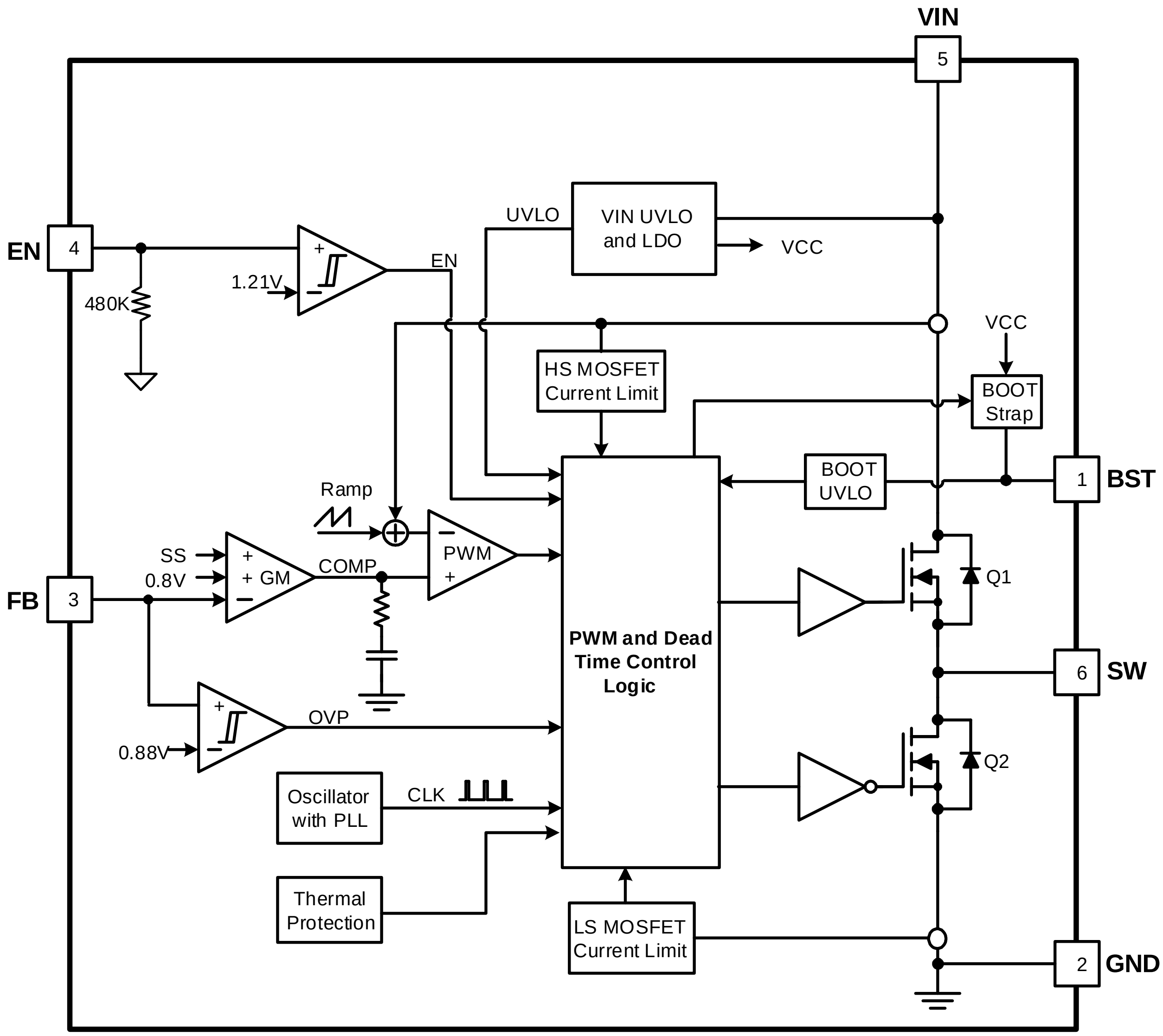


Figure 13. Functional Block Diagram

Overview

The SCT2411 device is 4.5V-40V input, 1A output, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 1.2MHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 1ms soft-start simplify the SCT2411 footprints and minimize the off-chip component counts. Meanwhile, it reduces the external passive components size as well.

The quiescent current of SCT2411 is 90uA typical under no-load and without switching condition. When disabling the device, the supply shut down current is only 1μA. The SCT2411 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition.

Peak Current Mode Control and Pulse Skipping Mode

The SCT2411 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2411 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 160mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss.

VIN Power

The SCT2411 is designed to operate from an input voltage supply range between 4.5V to 40V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

Enable and Under Voltage Lockout UVLO

The SCT2411 Under Voltage Lock Out (UVLO) default startup threshold is typical 4.3V with VIN rising and shutdown threshold is 3.86V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

When applying a voltage higher than the EN high threshold (typical 1.21V/rising), the SCT2411 enables all functions and the device starts soft-start phase. The SCT2411 has the built in 1ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/falling).

An internal 480k pull down resistor make EN pin floating shut down the SCT2411. For the application requiring higher VIN UVLO voltage than the default setup, connect an external resistor divider (R3 and R4) shown in Figure 14 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively If there is no requirement for the VIN UVLO program, connect the EN to VIN to simplify the external circuitry.

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

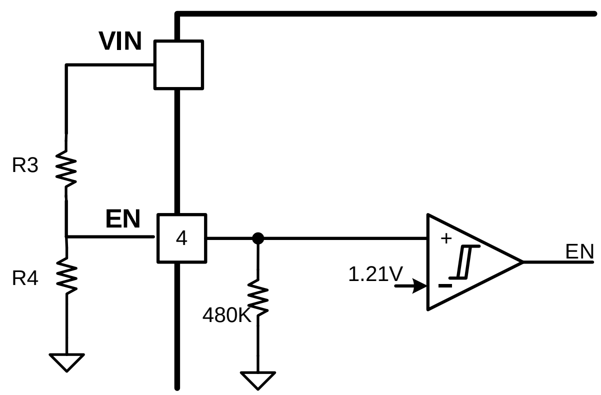


Figure 14. Adjustable VIN UVLO

$$V_{rise} = \frac{1.21 * R3(R4 + 480k)}{R4 * 480k} + 1.21 \quad (1)$$

$$V_{fall} = \frac{1.1 * R3(R4 + 480k)}{R4 * 480k} + 1.1 \quad (2)$$

Where:

V_{rise}: Vin rise threshold to enable the device
V_{fall} : Vin fall threshold to disble the device

Output Voltage

The SCT2411 regulates the internal reference voltage at 0.8V with ± 2.5% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Peak Current Limit

The SCT2411 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. The maximum current passing through the power MOSFET is limited cycle-by-cycle. The switching frequency folds back to prevent an inductor current run-away during start-up or short circuit.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2411 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Internal Soft-Start

The SCT2411 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 1ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets.
The soft-start also resets during shutdown due to thermal overloading.

Over Current Protection

The SCT2411 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition. The inductor current IL is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on.

As shown in Figure 15, when overload or hard short happens, once the high-side MOSFET Q1 current exceeds the HS limit, Q1 is turned off immediately and Q2 is turned on. If the low-side MOSFET Q2 current is higher than the LS current limit during Q2 ON time and next switching cycle will be skipped until Q2 current is lower than LS current limit. Then, Q1 is turned on and Q2 is turned off in another Over protection cycle until the overload or hard short is released.

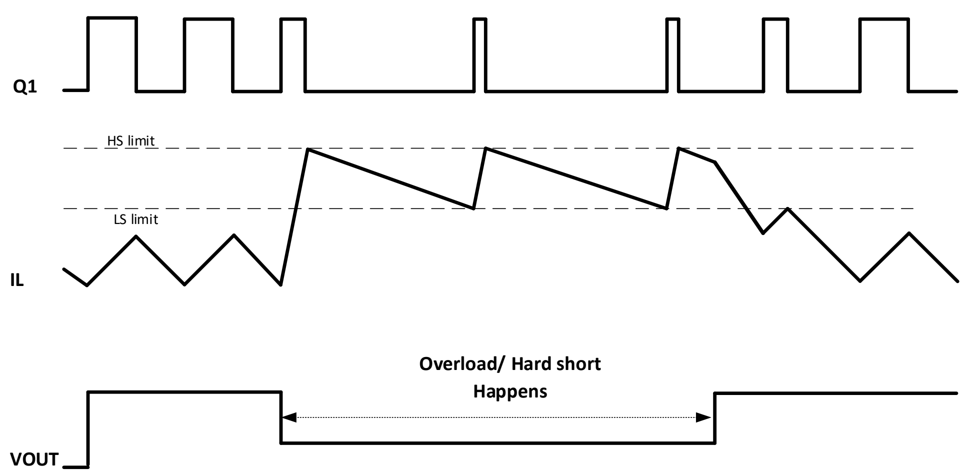


Figure 15. Over Current Protection

Over voltage Protection

The SCT2411 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

Once the junction temperature in the SCT2411 exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 145°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

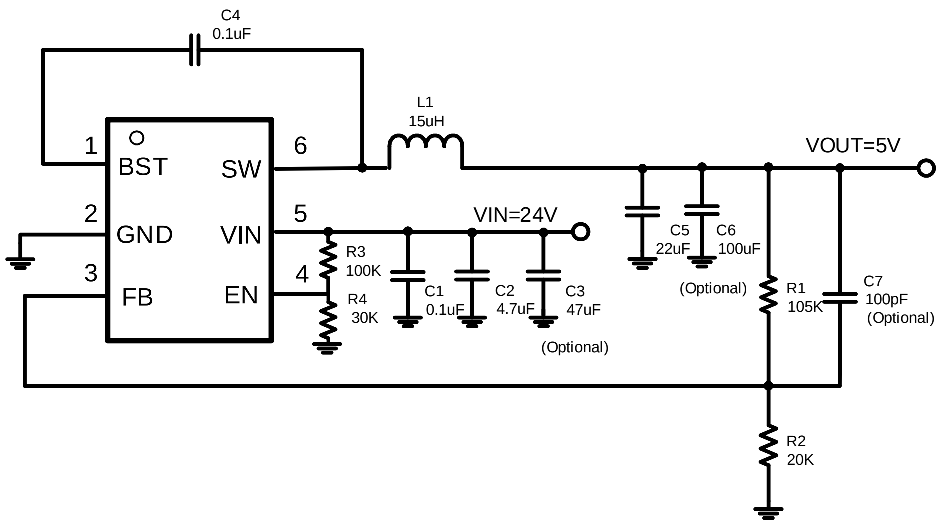


Figure 16. 24V Input, 5V/1A Output

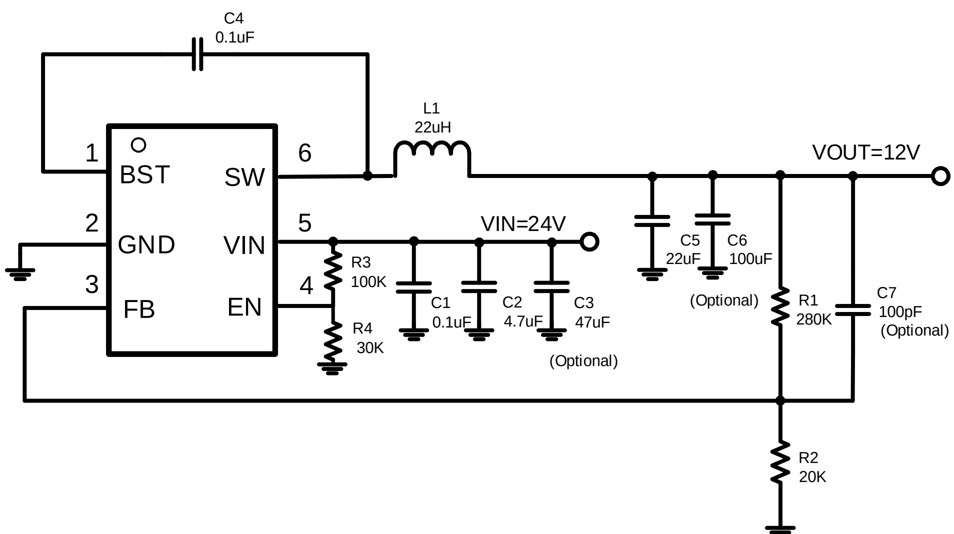


Figure 17. 24V Input, 12V/1A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Current	1A
Switching Frequency	1.2MHz
Start Input Voltage (rising VIN)	5.5V
Stop Input Voltage (falling VIN)	5V

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 20KΩ. Use Equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_1, R_2 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.8 V	24.9 KΩ	20 KΩ
2.5 V	42.2 KΩ	20 KΩ
3.3 V	62 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ
12 V	280 KΩ	20 KΩ

Under Voltage Lock-Out

An external voltage divider network of R3 from the input to EN pin and R4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.5V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 5V (stop or disable). Use Equation 5 and Equation 6 to calculate the values 100 kΩ and 30 kΩ of R3 and R4 resistor.

$$V_{rise} = \frac{1.21 * R3(R4 + 480k)}{R4 * 480k} + 1.21 \quad (5)$$

$$V_{fall} = \frac{1.1 * R3(R4 + 480k)}{R4 * 480k} + 1.1 \quad (6)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~30% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 7.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 8 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (8)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 9 and Equation 10.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \tag{9}$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \tag{10}$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 1.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 1.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2411 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

15uH inductor value is recommended for 5V output voltage and 22uH inductor is recommended for 12V output voltage.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 11.

$$\mathrm{I_{CINRMS}} = \mathrm{I_{OUT}} * \sqrt{\frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} * (1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}})} \tag{11}$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$\mathrm{I_{CINRMS}} = 0.5 * \mathrm{I_{OUT}} \tag{12}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \tag{13}$$

For this example, a 4.7μF, X7R ceramic capacitors rated of 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \tag{14}$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

Application Waveforms

V_{IN}=24V, V_{OUT}=5V, unless otherwise noted

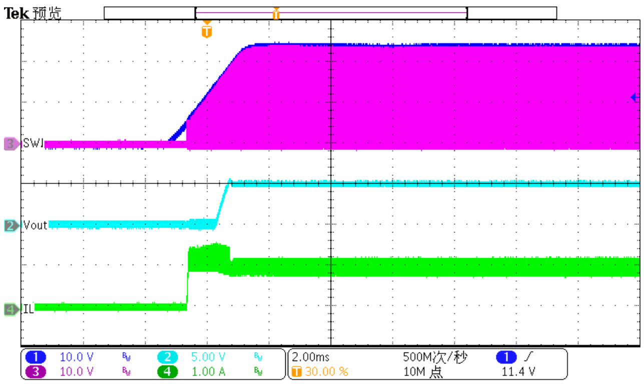


Figure 18. Power up (I_{LOAD}=1A)

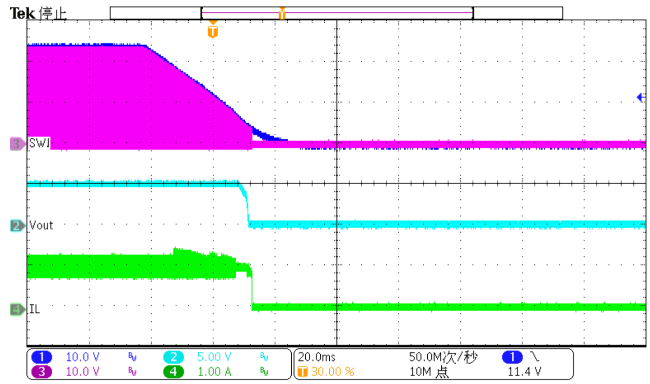


Figure 19. Power down (I_{LOAD}=1A)

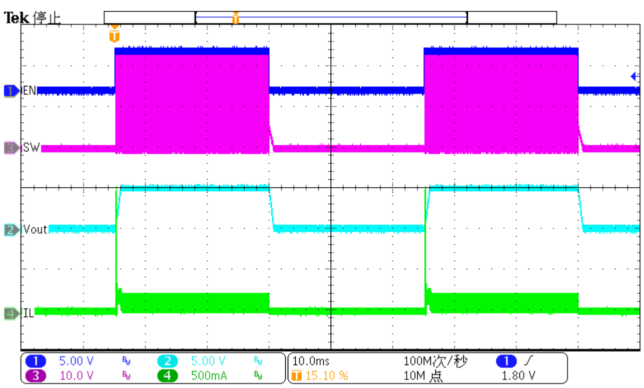


Figure 20. EN toggle (I_{LOAD}=0.01A)

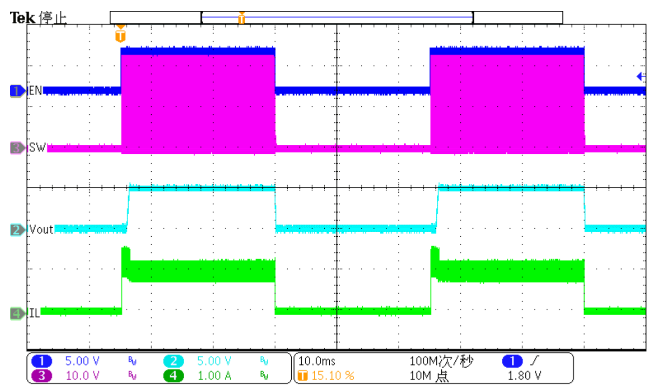


Figure 21. EN toggle (I_{LOAD}=1A)

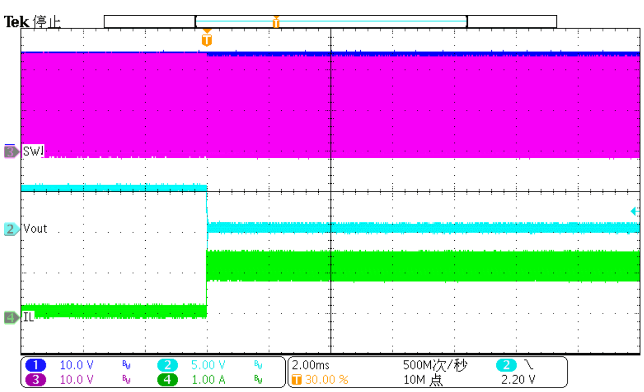


Figure 22. Over Current Protection (0.1A to hard short)

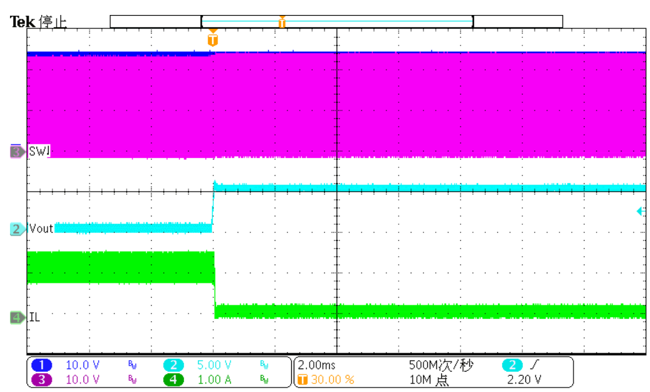


Figure 23. Over Current Release (hard short to 0.1A)

Application Waveforms

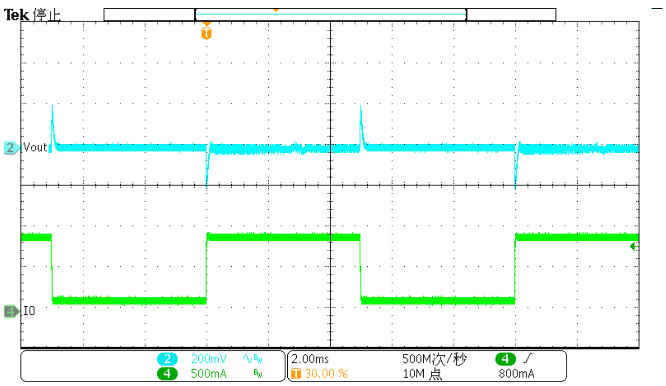


Figure 24. Load Transient (0.1A-0.9A, 1.6A/us)

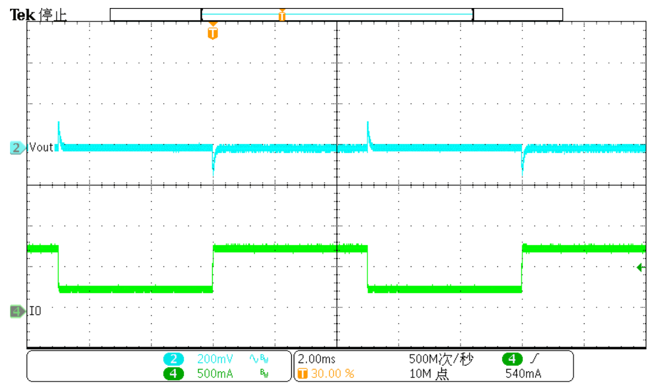


Figure 25. Load Transient (0.25A-0.75A, 1.6A/us)

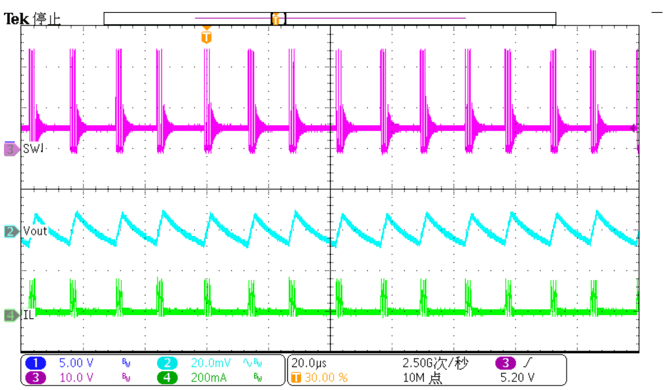


Figure 26. Output Ripple (I_{LOAD}=10mA)

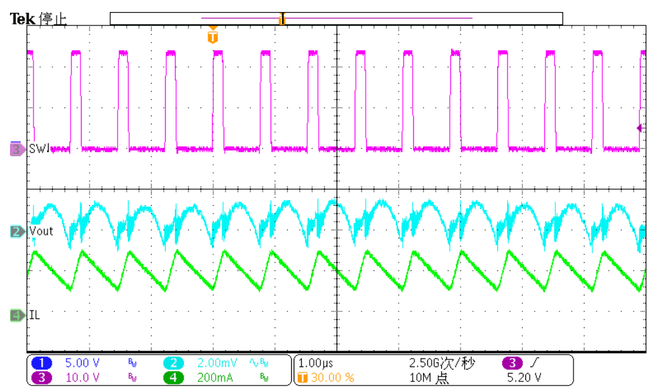


Figure 27. Output Ripple (I_{LOAD}=0.2A)

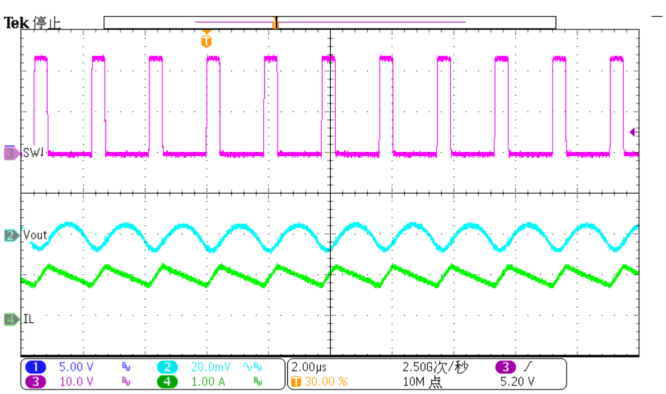


Figure 28. Output Ripple (I_{LOAD}=1A)

Figure 29. Thermal, 24V_{IN}, 5V_{OUT}, 0.8A

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential.

1. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling.
2. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

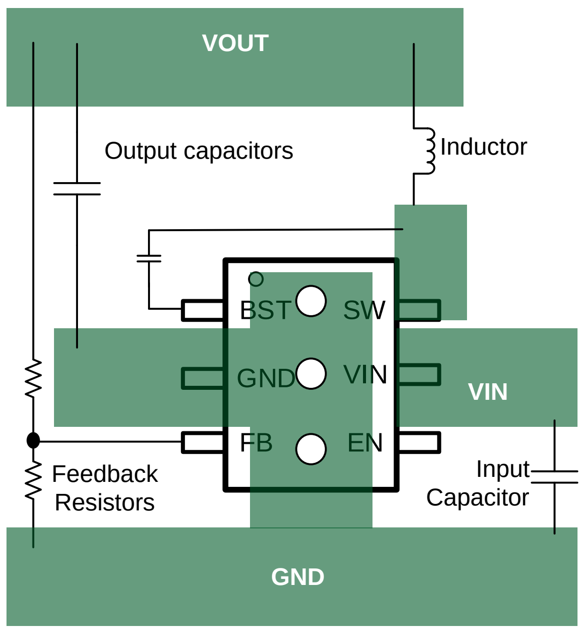
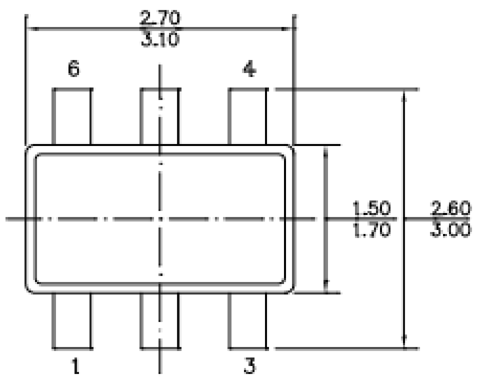
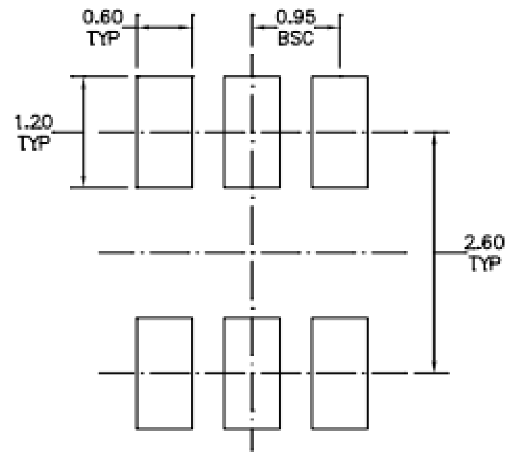


Figure 30. PCB Layout Example

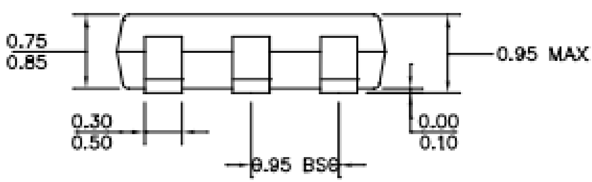
PACKAGE INFORMATION



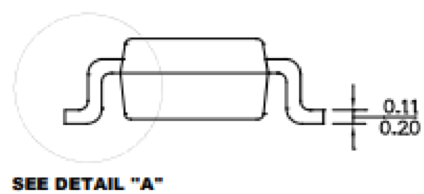
TOP VIEW



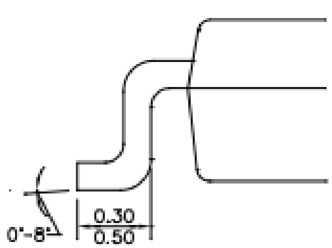
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

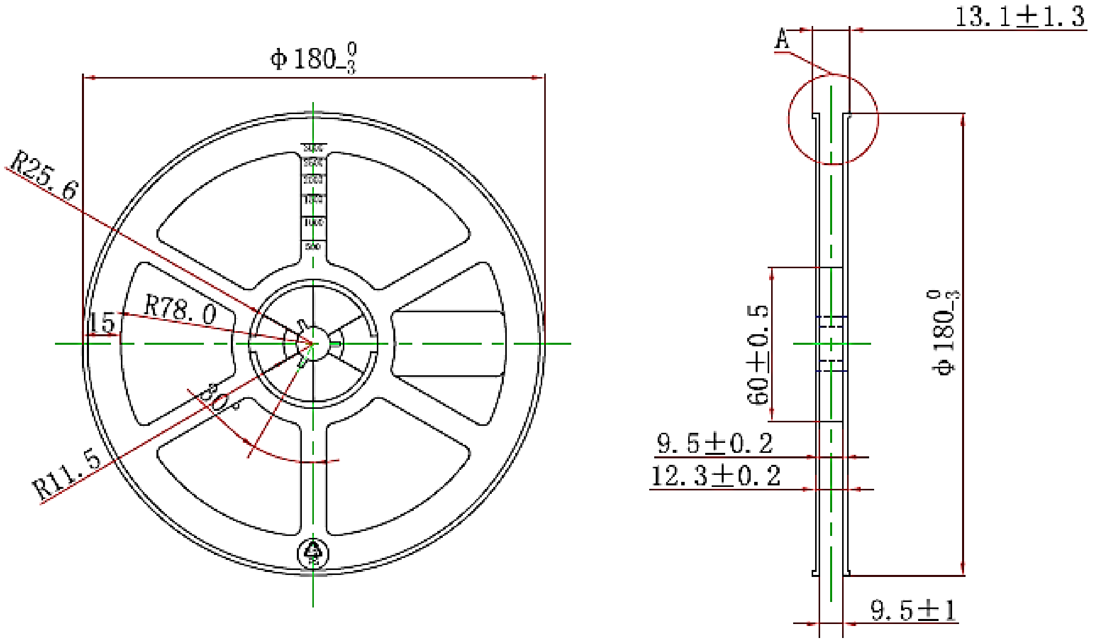


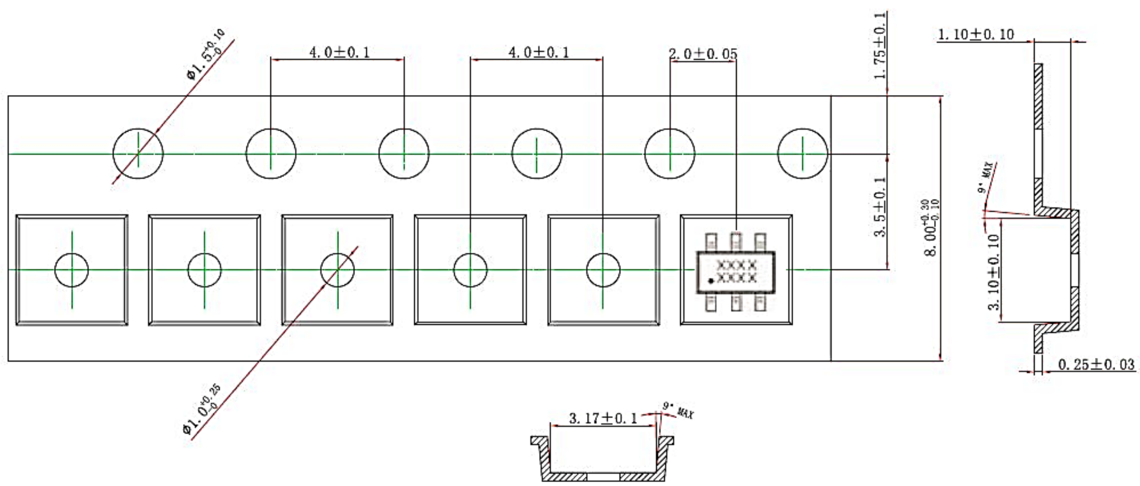
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

TAPE AND REEL INFORMATION





Feeding Direction

