2.8V-5.5V Vin 2A Synchronous Step Down Convertor

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Input Voltage Range: 2.8V-5.5V
- Up to 2A Peak Output Current
- Low Shutdown Current 0.05uA
- Low Quiescent operating Current: 38uA
- 0.6V Feedback Reference Voltage
- 1.5MHz Switching Frequency
- Integrated 80mΩ High-Side and 50mΩ Low-Side Power MOSFETs
- 100% Duty Cycle Mode
- Adjustable output voltage from 0.6 V to 5 V
- Active output discharge
- 1.5ms Internal Soft-start Time
- Power Good Indicator
- Integrated Protection Feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - HICCUP Over load Protection
  - Thermal Shutdown Protection:160°C
- QFN-8L1.5mm*2mm Package
- Available in a Wettable Flank Package

APPLICATIONS

- Automotive Infotainment
- Battery-Powered Devices
- Solid state driver
- Automotive Infotainment

DESCRIPTION

The SCT2120Q is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. The device achieves 2A of peak output current from a 2.8V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V

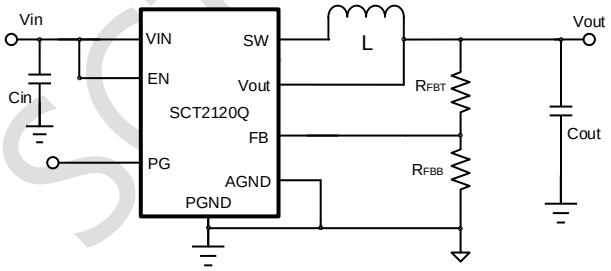
Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The SCT2120Q operates in power saving mode, which maintains high efficiency during light load operation.

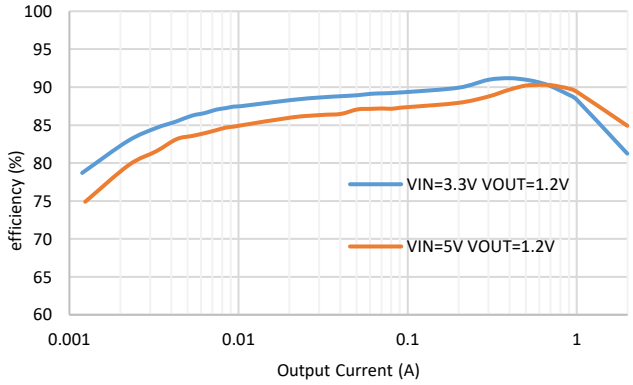
It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2120Q requires a minimal number of external components and is available in a space-saving QFN-8L1.5mm*2mm package.

TYPICAL APPLICATION



Typical Application



Efficiency OUT=1.2V

REVISION HISTORY

Revision 0.8: Customer Sample

Revision 0.81: Update EC table

Revision 0.82: Update RECOMMENDED OPERATING CONDITIONS TJ&TA Range

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2120QFTA	2120Q	QFN-8L1.5mm*2mm

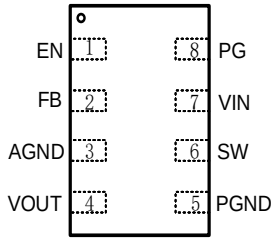
1) For Tape & Reel, Add Suffix R (e.g. SCT2120QFTAR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, PG, VOUT, SW,FB	-0.3	6	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: QFN-8L 1.5mm x 2mm, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
EN	1	Enable logic input. Connect high to enable device
FB	2	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage
AGND	3	Analog Ground pin
VOUT	4	Output Pin and discharge pin
PGND	5	Power Ground pin
SW	6	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time.
VIN	7	Power supply input pin
PG	8	Power-good indicator. The output of PG is an open drain that connects to VIN via an internal pull-up resistor. PG goes high if the output voltage is within ±10% of the nominal voltage.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.8	5.5	V
V_{OUT}	Output voltage range	0.6	5	V
T_A	Operating ambient temperature	-40	125	°C
TJ	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	90.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.77	
Ψ_{JB}	Junction-to-board characterization parameter(1)	10.7	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	124.4	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	10.9	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2120Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2120Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.8		5.5	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.7		V
	Hysteresis			200		mV
I_{SD}	Shutdown current			50		nA
I_Q	Quiescent current from VIN	no load, no switching		38		uA
V_{FB}	Reference voltage of FB	Tj=25 °C	0.594	0.6	0.606	V
		Tj=-40°C ~125 °C	0.591		0.609	
I_{FB}	FB pin leakage current				80	nA
Power switch						
R_{HS}	High-side switch on resistance			80		mΩ
R_{LS}	Low-side switch on resistance			50		mΩ
$ILIM_{HS}$	High-side peak current limit			3.5		A
$ILIM_{LS}$	Low-side peak current limit			3		A
Soft start						
T_{SS}	Soft-start Time			1.5		mS
EN & PG						
V_{ENH}	High-level Threshold voltage		1.2			V
V_{ENL}	Low- level Threshold voltage				0.4	V
R_{EN}	EN Pull down resistance			1.33		MΩ
R_{DIS}	Output Discharge resistance			150		Ω
V_{PGTL}	Power Good Lower Threshold voltage	FB rinsing(Reference to V_{FB})		95		%
		FB falling(Reference to V_{FB})		90		%
V_{PGTH}	Power Good Upper Threshold voltage	FB rinsing(Reference to V_{FB})		110		%
		FB falling(Reference to V_{FB})		105		%
I_{PG_SINK}	Power Good Sink Current Capability	VPG=0.4A		1		mA
R_{PG}	Power Good Internal Pull up resistor			550		KΩ
T_{PGD}	Power Good Delay			100		uS
Switching Frequency						
F_{SW}	Switching frequency	Vin=5V,Vout=1.2V,CCM		1.5		MHz
t_{ON_MIN}	Minimum on-time			80		ns
t_{OFF_MIN}	Minimum off-time			100		ns
Protection						
T_{SD}	Thermal shutdown threshold			160		°C
	Hysteresis			20		°C

TYPICAL CHARACTERISTICS

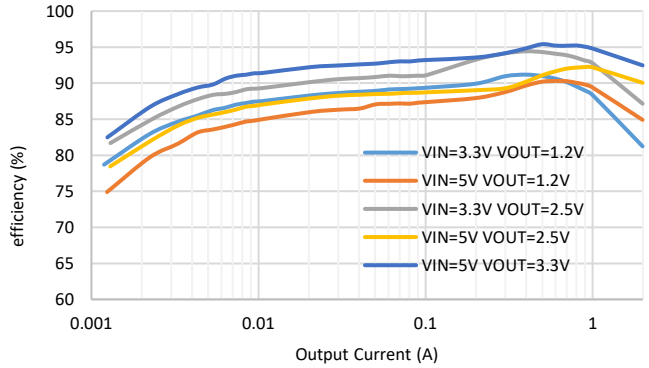


Figure 1. Efficiency vs Load Current

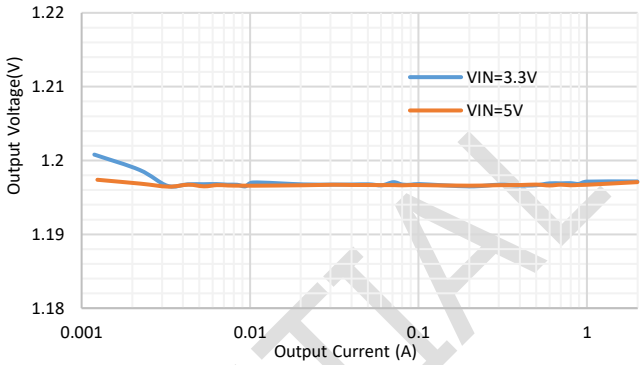


Figure 2. Load Regulation

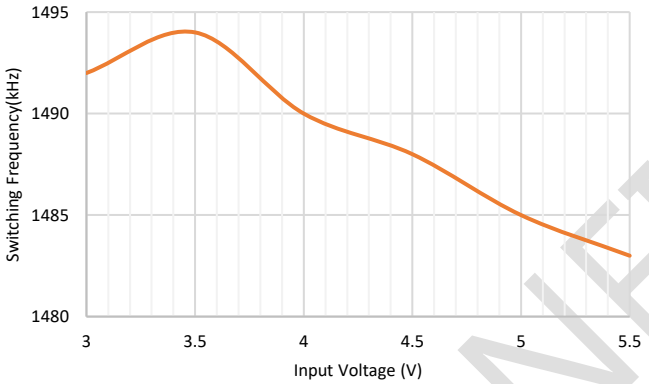


Figure 2. Frequency VS Input Voltage

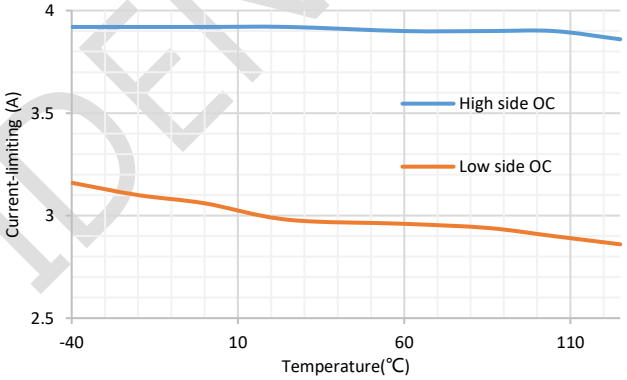


Figure 4. Current-limiting VS Temperature

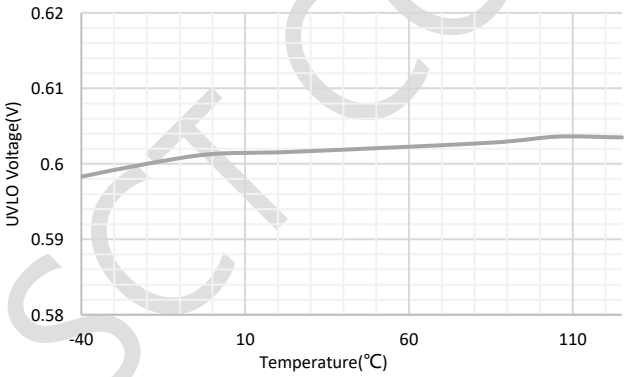


Figure 5. V_{FB} vs Temperature

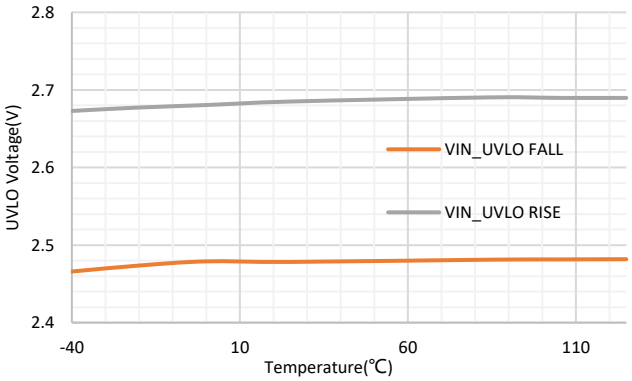


Figure 6. UVLO vs Temperature

FUNCTIONAL BLOCK DIAGRAM

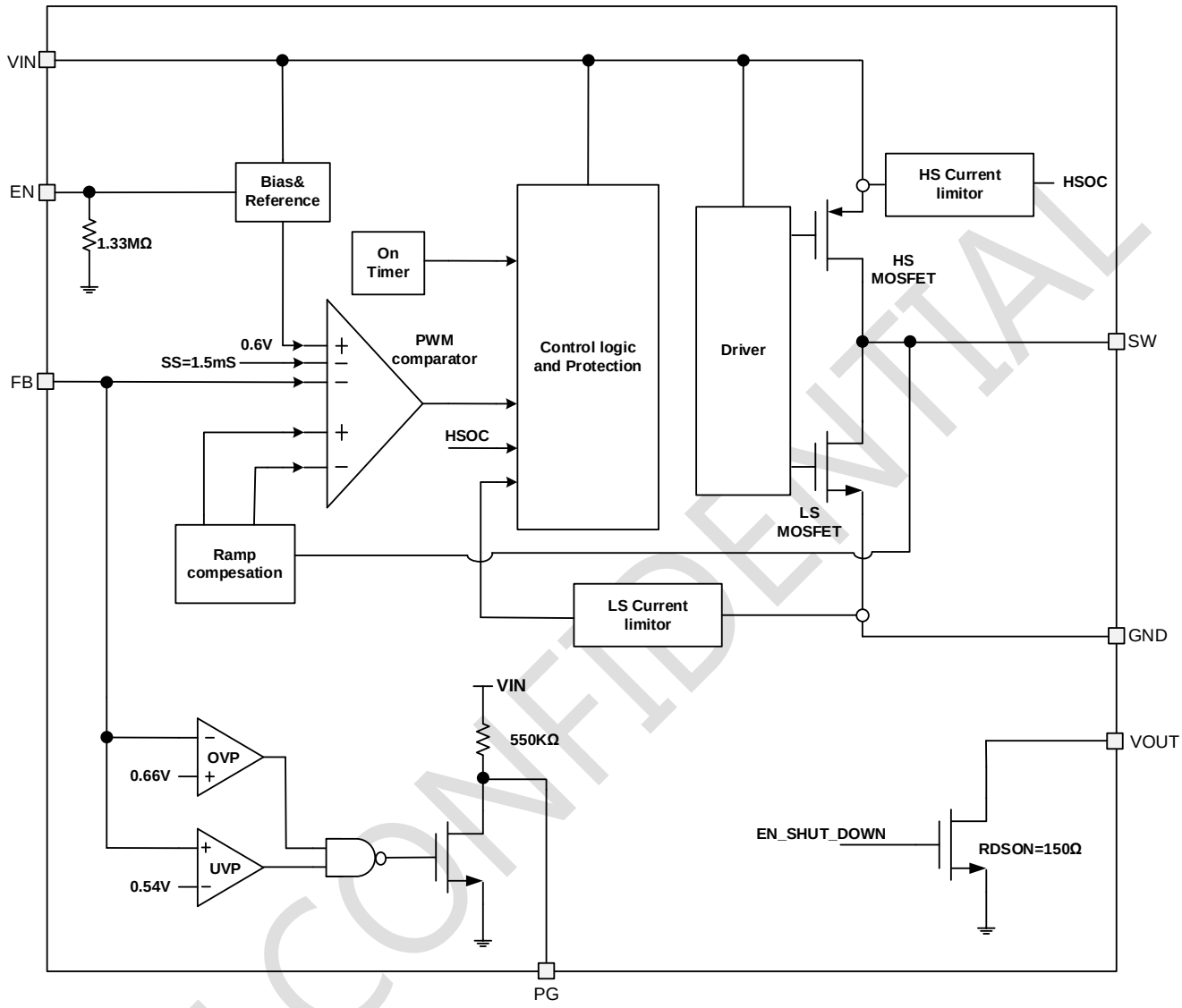


Figure 7. Functional Block Diagram

OPERATION

Overview

The SCT2120Q is a 2.8V-5.5V input, 2A output, synchronous buck converter with built-in 80mΩ high-side and 50mΩ low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The device operates in Pulse Frequency Modulation (PFM) mode at light loading to provides high light load efficiency. The quiescent current is typically 38uA under no load or sleep mode condition to achieve high efficiency at light load.The SCT2120Q features an internal 1.2ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The SCT2120Q has a default input start-up voltage of 2.7V with 200mV hysteresis.

Constant On-time Control

The SCT2120Q device is 2.8-5.5V input, 2A output, synchronous step-down converters with internal power MOSFETs. Constant on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT2120Q turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2120Q turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times F_{SW}} \quad (1)$$

Where:

- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- F_{SW} is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.6V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 100ns typical.

100% Duty Cycle Mode

The SCT2120Q has a 100% duty cycle mode. When the input voltage gradually approaches the output voltage, the duty cycle is large and reaches the minimum turn off time (100nS), the switching frequency of the output voltage begins to decrease. When the input voltage drops to the same level as the output voltage, the high side MOSFET remains constant on.

Power Saving Mode (PSM)

The SCT2120Q is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only

by output capacitor, when FB voltage is lower than 0.6V, the next ON cycle begins. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- T_{ON} is on-time.
- L is the inductance of inductor.

Output Voltage

The SCT2120Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FBT} = (\frac{V_{OUT}}{V_{REF}} - 1) \times R_{FBB} \quad (3)$$

Where:

- V_{OUT} is the output voltage.
- V_{REF} is the reference voltage.
- R_{FBT} is the resistor connecting the output to the FB pin.
- R_{FBB} is the resistor connecting the FB pin to the ground.

Under Voltage Lockout UVLO

The SCT2120Q Under Voltage Lock Out (UVLO) default startup threshold is typical 2.7V with VIN rising and shutdown threshold is 2.5V with VIN falling.

Enable(EN)

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.4V), the chip shuts down. Force EN above its rising threshold voltage (1.2V) to turn the part on. Leave EN floating or pull it down to ground to disable the SCT2120Q. There is an internal 1.5MΩ resistor connected from the EN pin to ground. When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor**.**

Soft Start(SS)

The SCT2120Q has a build in soft start that ramps up the output voltage in a controlled slew rate avoiding overshoot at startup. The soft start time is about 1.5ms typical.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period

and the low-side MOSFET during the OFF period. When the inductor current (I_L) reaches the high-side MOSFET peak current limit (typically 3.5A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on, and stays on until I_L drops below the low-side MOSFET valley current limit (typically 3A). If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

Power Good Indicator

The SCT2120Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is an open drain of an internal pullup resistor 550KΩ. When FB is within ±10% of the regulation voltage (0.6V), PG is pulled up to VIN by the internal resistor. If the FB voltage is outside the ±10% window, PG is pulled to ground by an internal MOSFET.

Over voltage Protection

The SCT2120Q implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When the feedback voltage rises higher than 110% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on until trigger negative current limit or FB below reference voltage. Then HS-FET turns on with normal ON-time and turn off, following with a LS-FET on until negative current limited triggered or FB lower than reference voltage. The device exits this regulation period when the feedback voltage falls below 105% of the reference voltage.

Thermal Shutdown

Once the junction temperature in the SCT2120Q exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

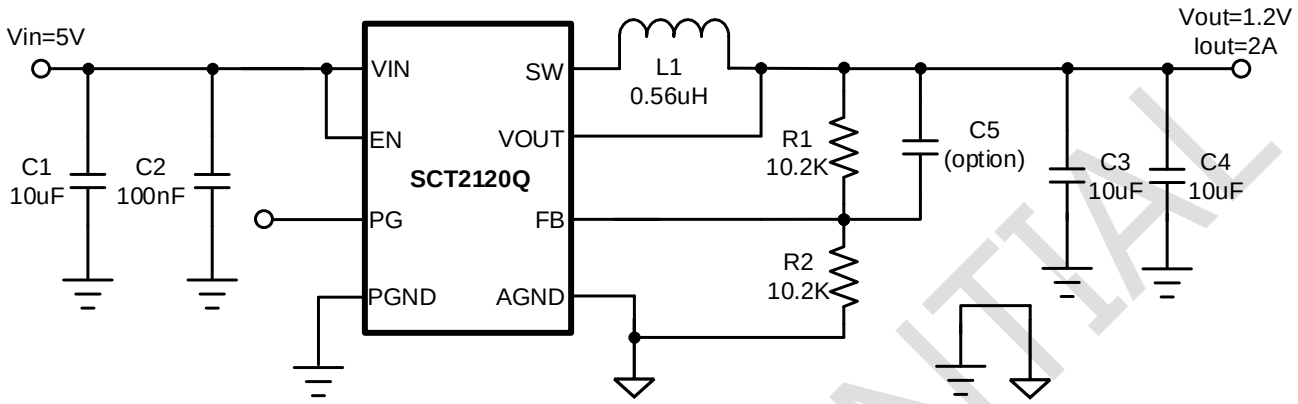


Figure 8. SCT2120Q Design Example, 1.2V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.8V to 5.5V
Output Voltage	1.2V
Maximum Output Current	2A
Switching Frequency	1.5MHz
Output voltage ripple (peak to peak)	2mV
Transient Response 0.2A to 1.8A load step	ΔVout =100mV

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2KΩ. Use equation 4 to calculate R1.

$$R1 = (\frac{V_{OUT}}{V_{REF}} - 1) \times R2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.2 V	10.2 KΩ	10.2 KΩ
1.8 V	20 KΩ	10.2 KΩ
2.5 V	32.4 KΩ	10.2 KΩ
3.3 V	46.5 KΩ	10.2 KΩ

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 5.

$$I_{LPP} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times F_{SW}} \quad (5)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- F_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 6 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{OUT(max)} \times LIR \times F_{SW} \times V_{IN(max)}} \quad (6)$$

Where:

- L_{MIN} is the minimum inductance required.
- F_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and

RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 7 and equation 8.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (7)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times (I_{LPP})^2} \quad (8)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 3.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 3.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2120Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 9.

$$I_{CINRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = \frac{I_{OUT}}{2} \quad (10)$$

Where:

- I_{CINRMS} is the RMS current in the input capacitor.
- I_{OUT} is the DC load current.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 11 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{F_{SW} \times C_{IN} \times V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where:

- ΔV_{IN} is the input voltage ripple.
- F_{SW} is the switching frequency.
- C_{IN} is the input capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

For this example, 10μF, X7R ceramic capacitors rated for 10 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 12 desired.

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times C_{OUT} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- F_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10μF ceramic output capacitors work for most applications.

Table 2: Component List with Typical Output Voltage BOM list

Vout	L1	COUT	R1	R2	C6
1.2V	0.56uH	20uF	10.2K	10.2K	option
1.8V	0.68uH	20uF	20K	10.2K	option
2.5V	1uH	20uF	32.4K	10.2K	option

Application Waveforms

V_{IN}=5V, V_{OUT}=1.2V, unless otherwise noted

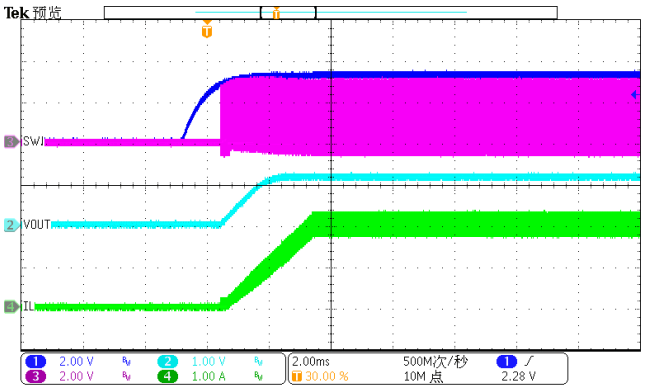


Figure 9. Power up (I_{LOAD}=2A)

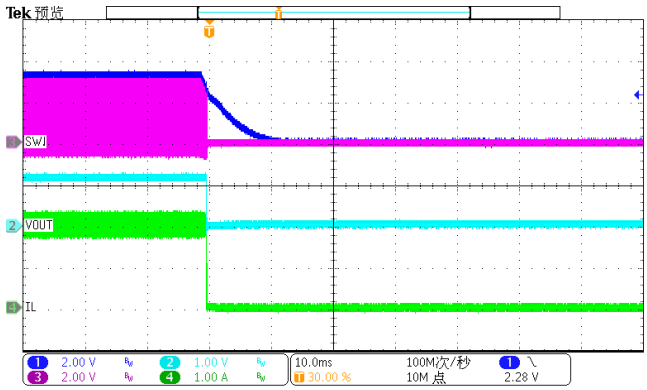


Figure 10. Power down (I_{LOAD}=2A)

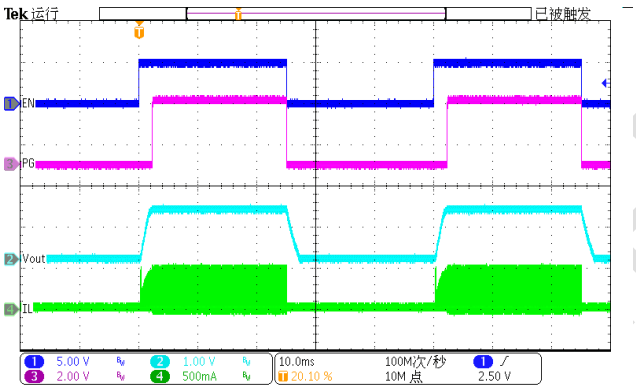


Figure 11. EN toggle (I_{LOAD}=10mA)

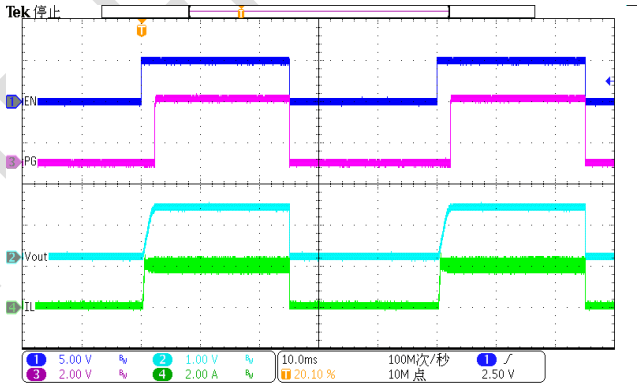


Figure 12. EN toggle (I_{LOAD}=2A)

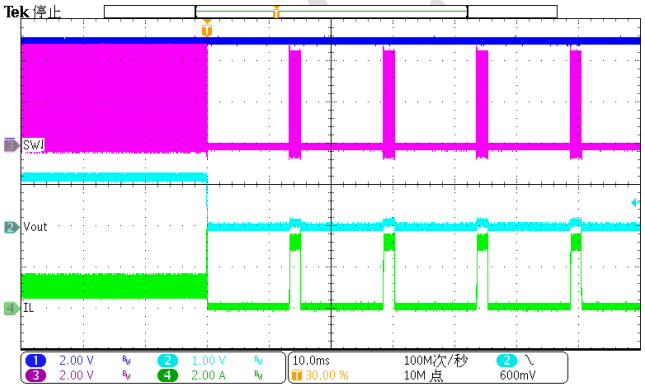


Figure 13. Over Current Protection (1A to hard short)

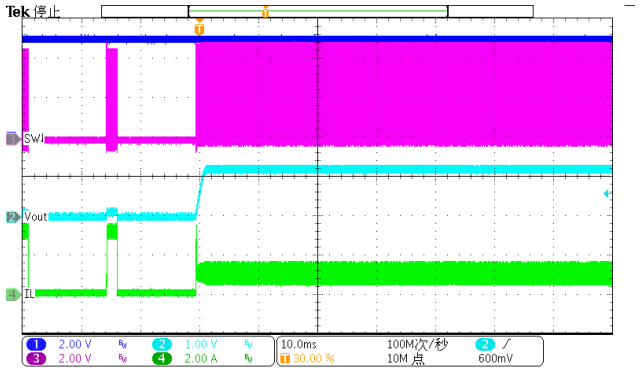


Figure 14. Over Current Release (hard short to 1A)

Application Waveforms

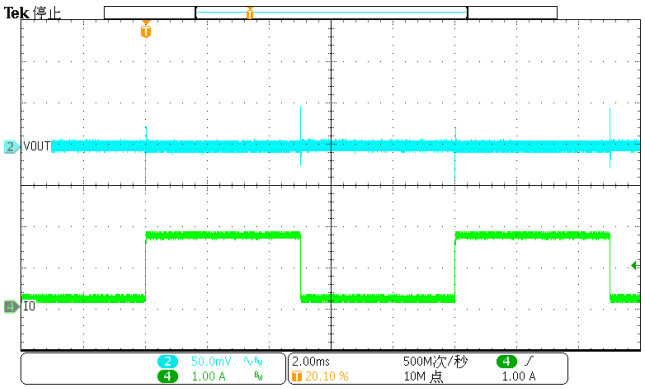


Figure 15. Load Transient (0.2A-1.8A, 1.6A/us)

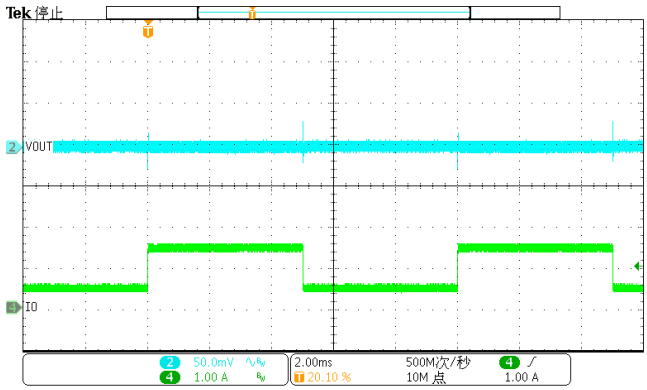


Figure 16. Load Transient (0.5A-1.5A, 1.6A/us)

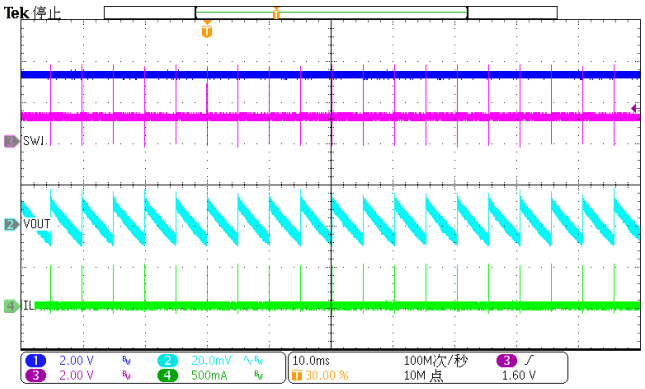


Figure 17. Output Ripple (I_{LOAD}=0A)

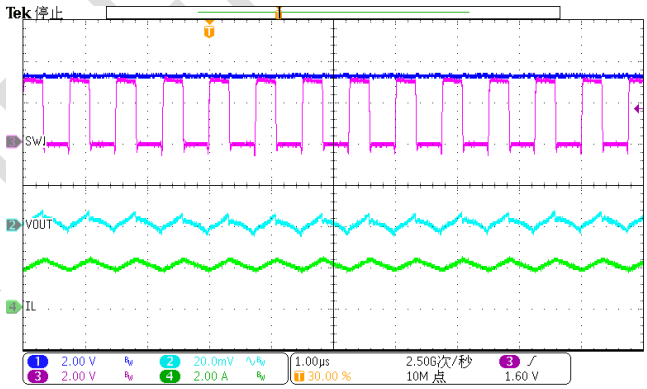


Figure 18. Output Ripple (I_{LOAD}=2A)

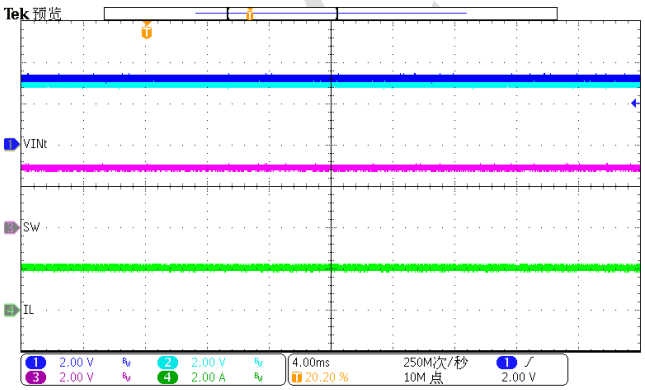


Figure 19. 100% Duty (VIN=3.3V,VOUT=3.3V,I_{LOAD}=2A)

Figure 20. Thermal, V_{IN}=5V, V_{OUT}=1.2V, I_O=2A

Layout Guideline

Proper PCB layout is a critical for SCT2120Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Route BST capacitor trace on the bottom layer to provide wide path for topside ground.

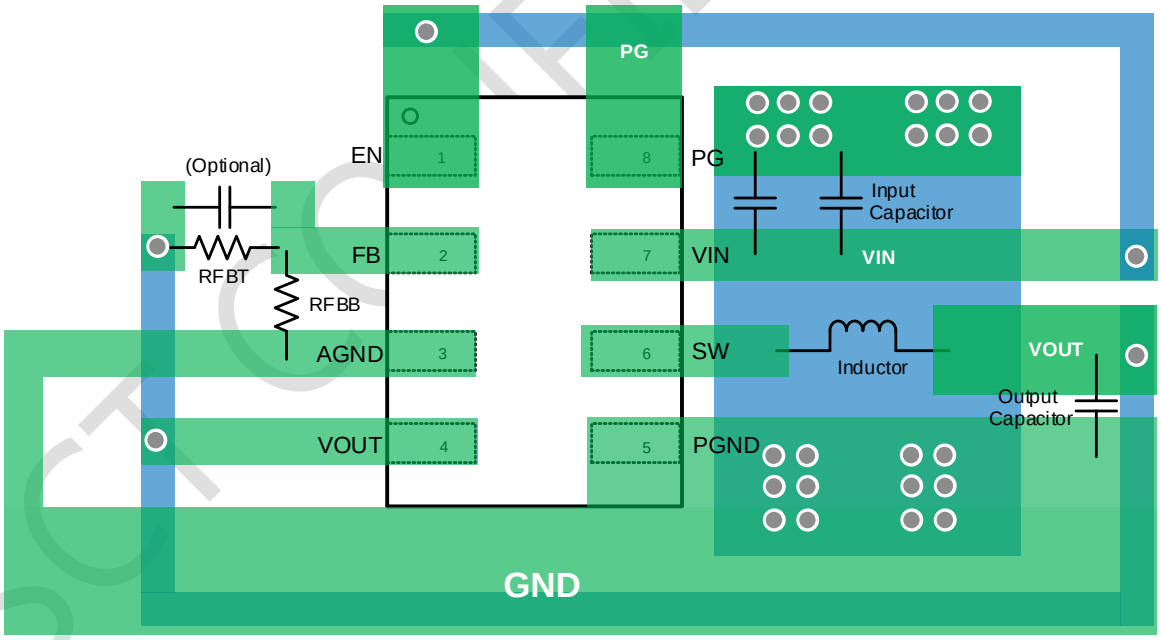
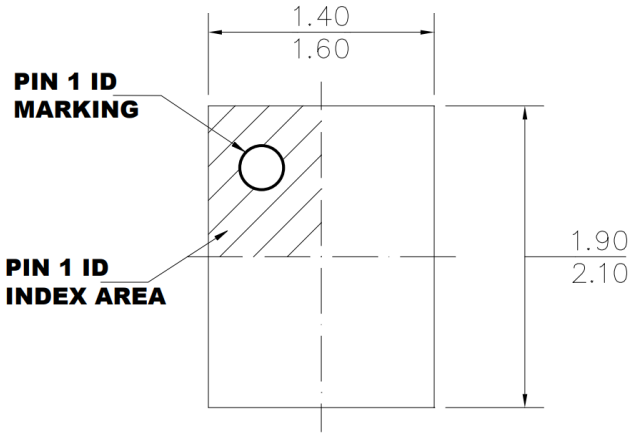
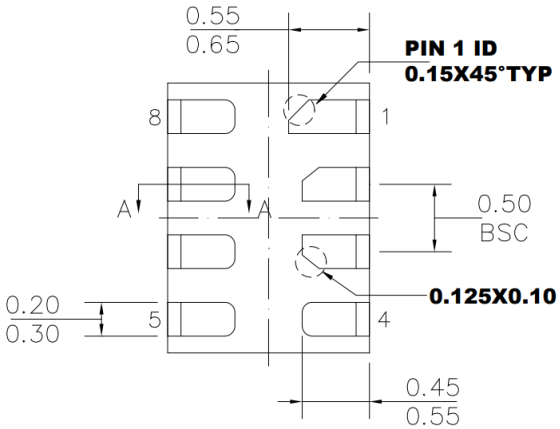


Figure 21. PCB Layout Example

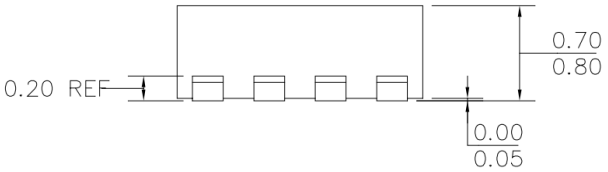
PACKAGE INFORMATION



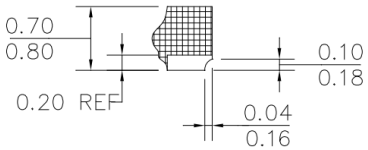
TOP VIEW



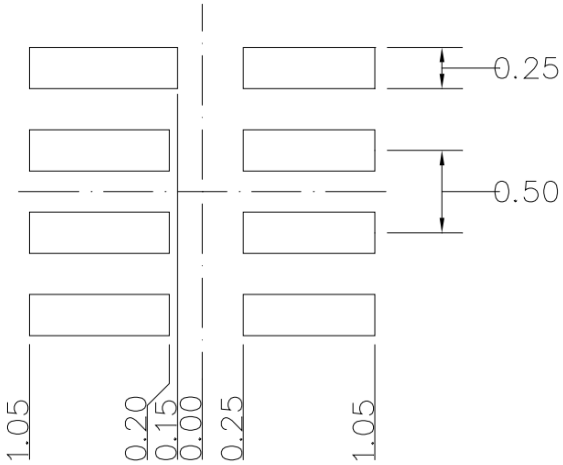
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

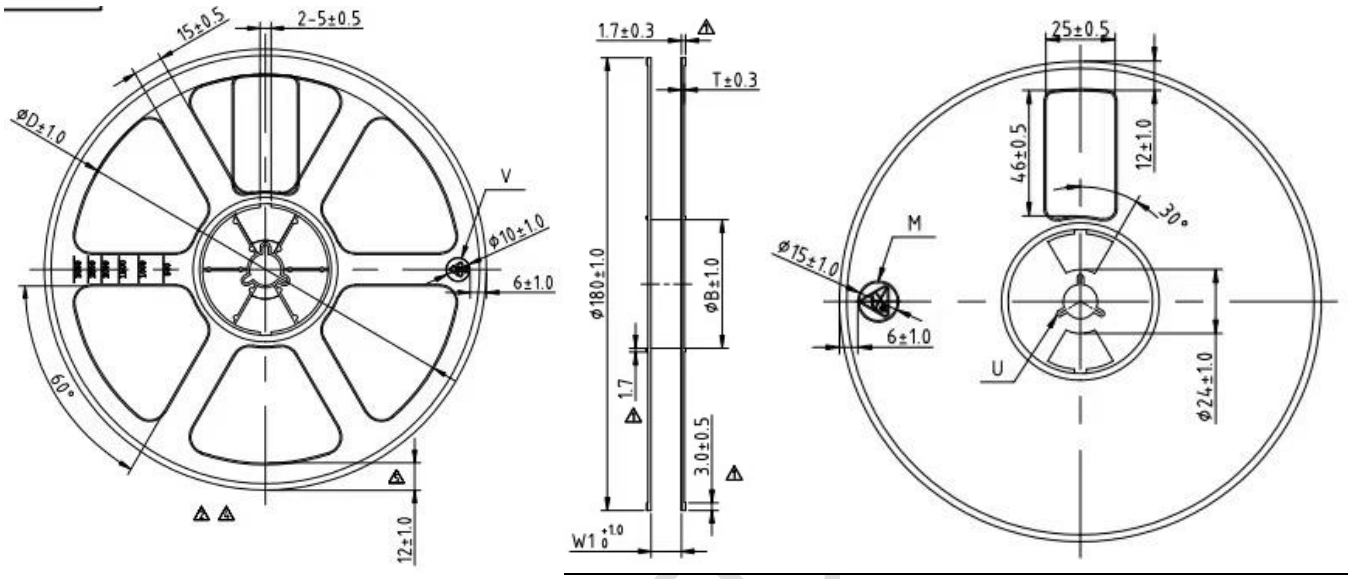
QFN-8L (1.5*2) Package Outline Dimensions

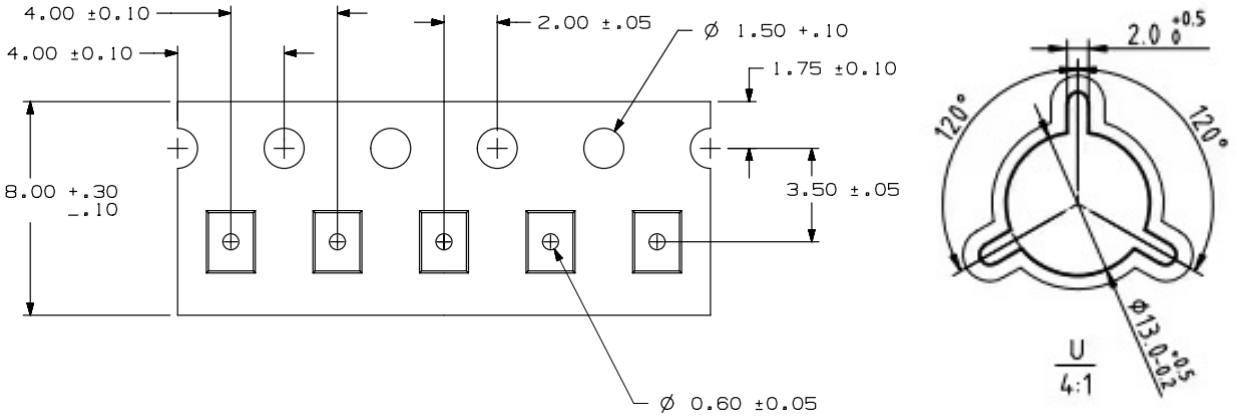
NOTE:

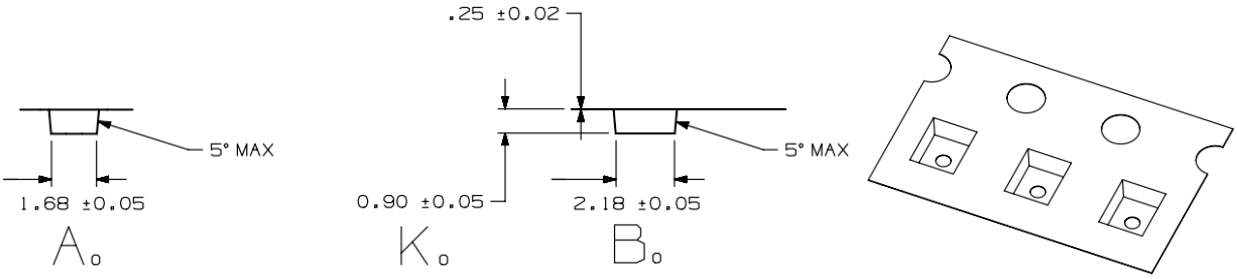
1. THE LEAD SIDE IS WETTABLE.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT2120QFTAR	QFN 1.5mmx2mm	8	3000







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